

FIG. 1A

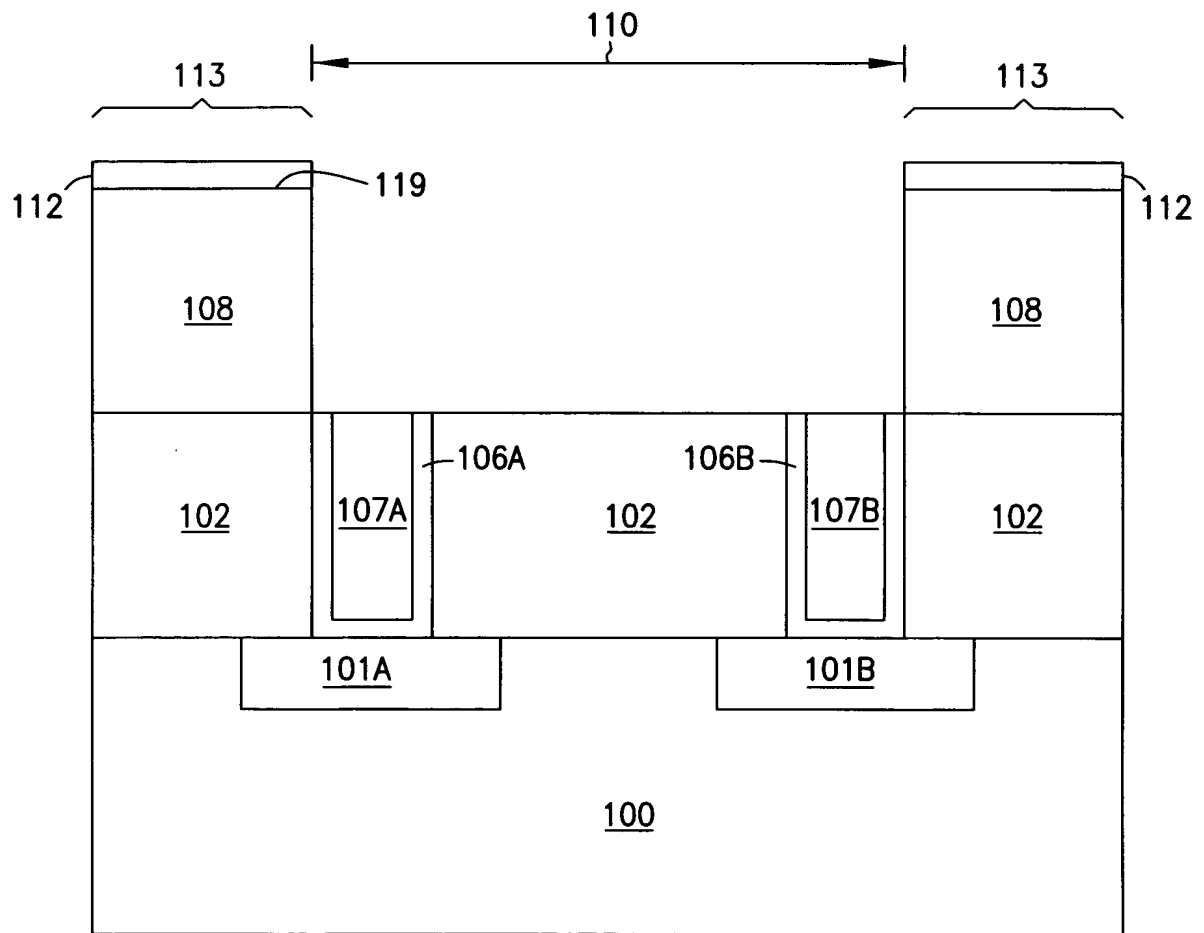


FIG. 1B

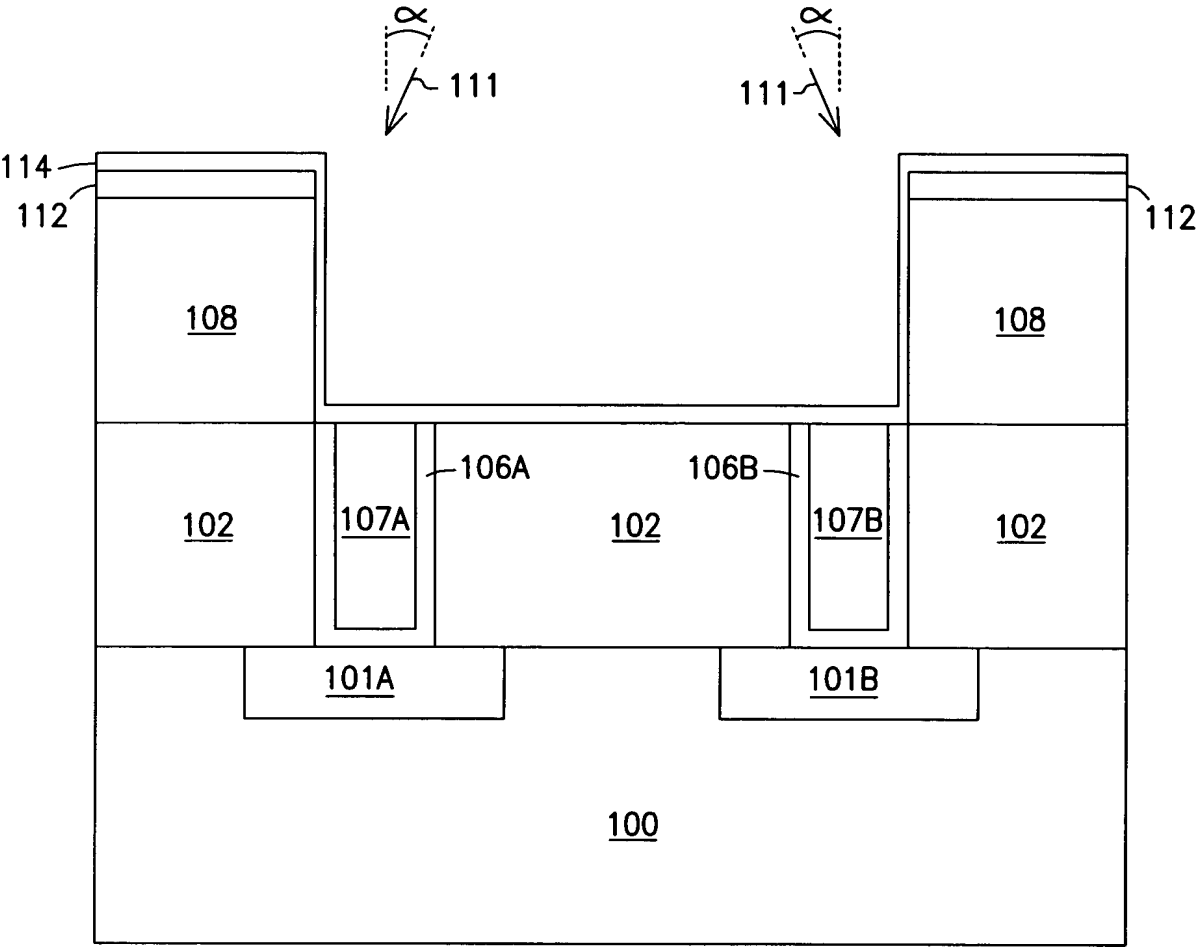


FIG. 1C



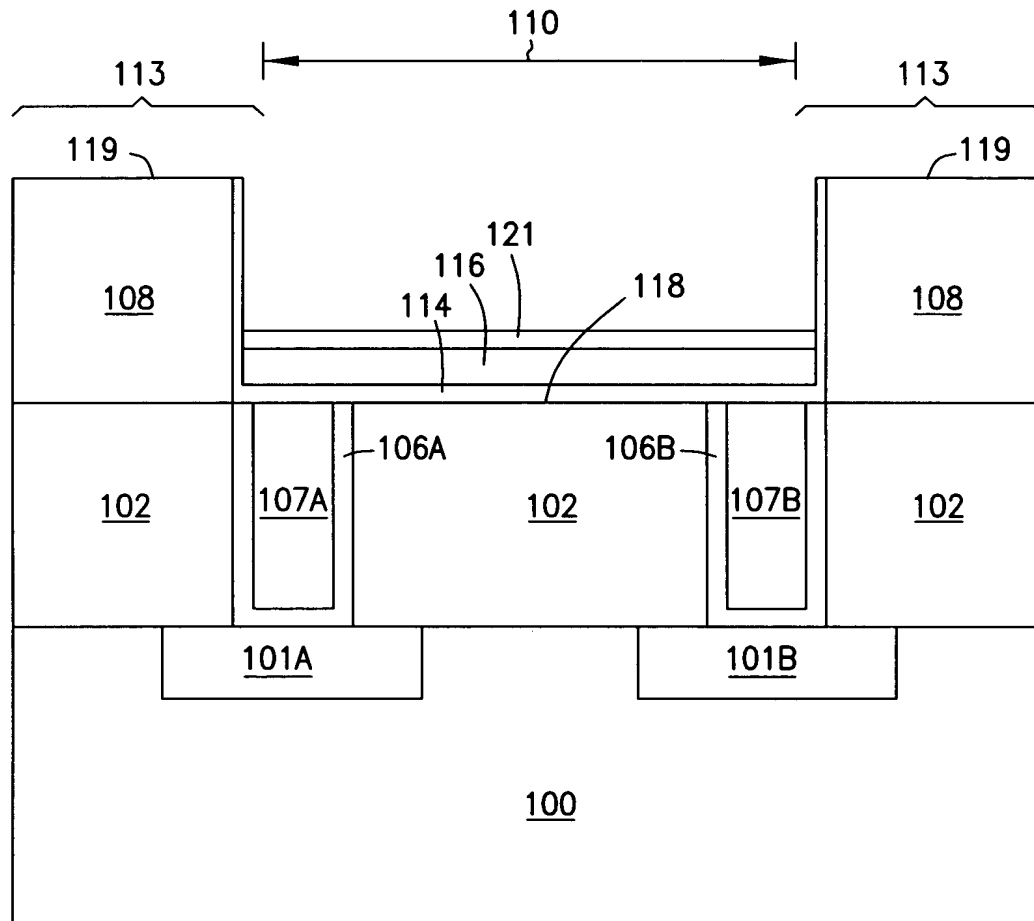


FIG. 1E

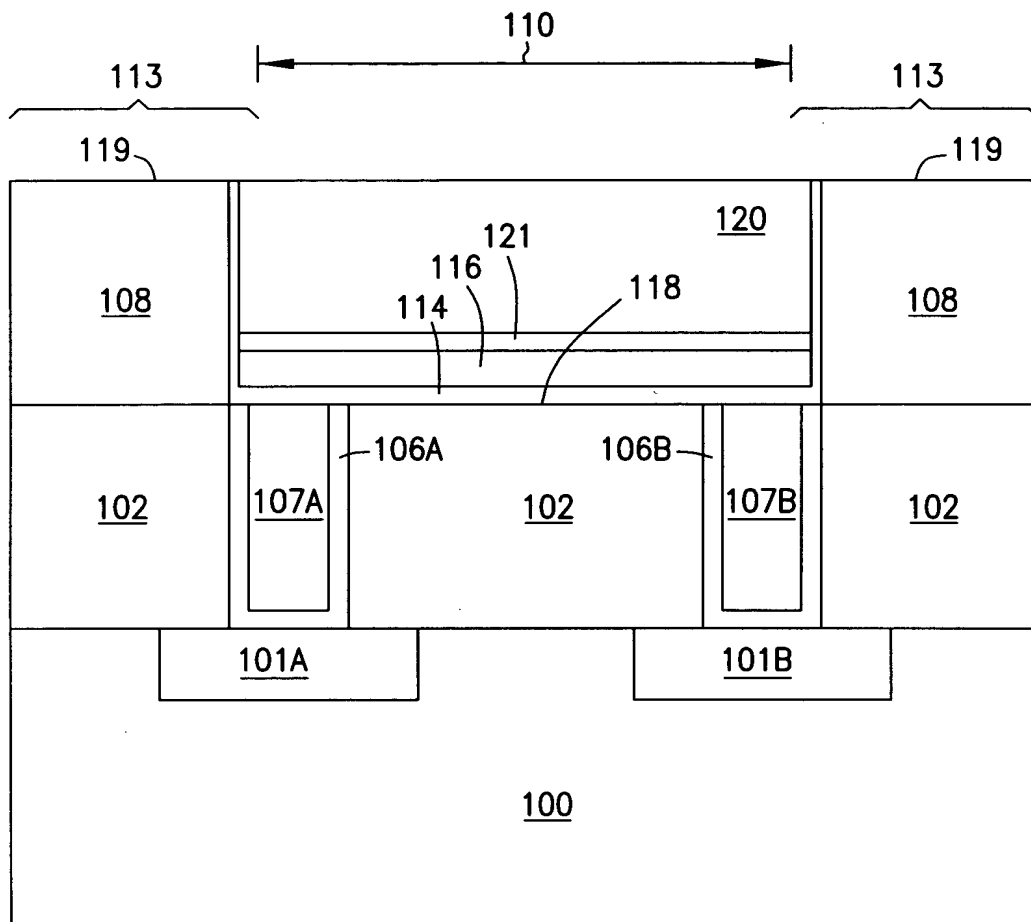


FIG. 1F

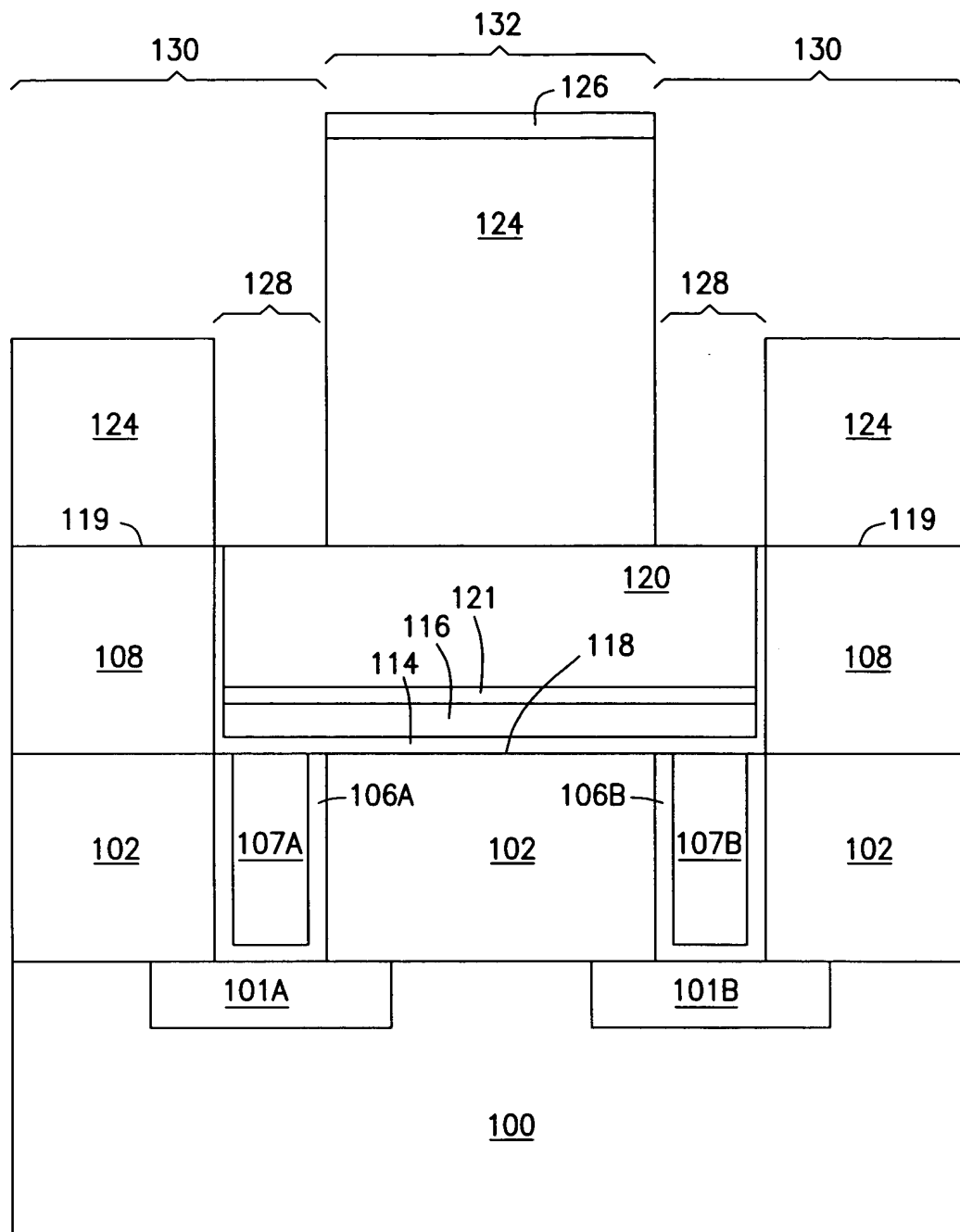


FIG. 1G

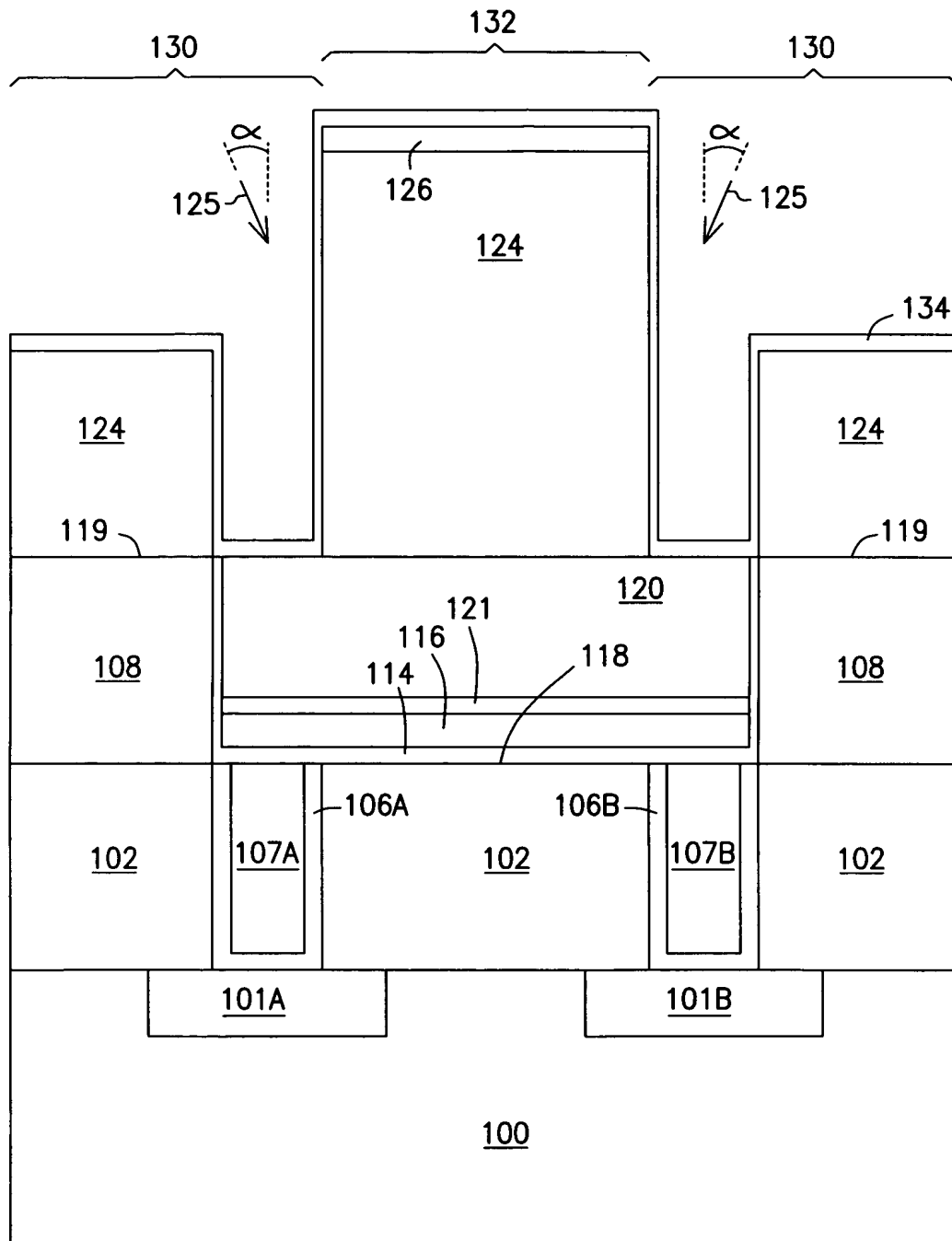


FIG. 1H



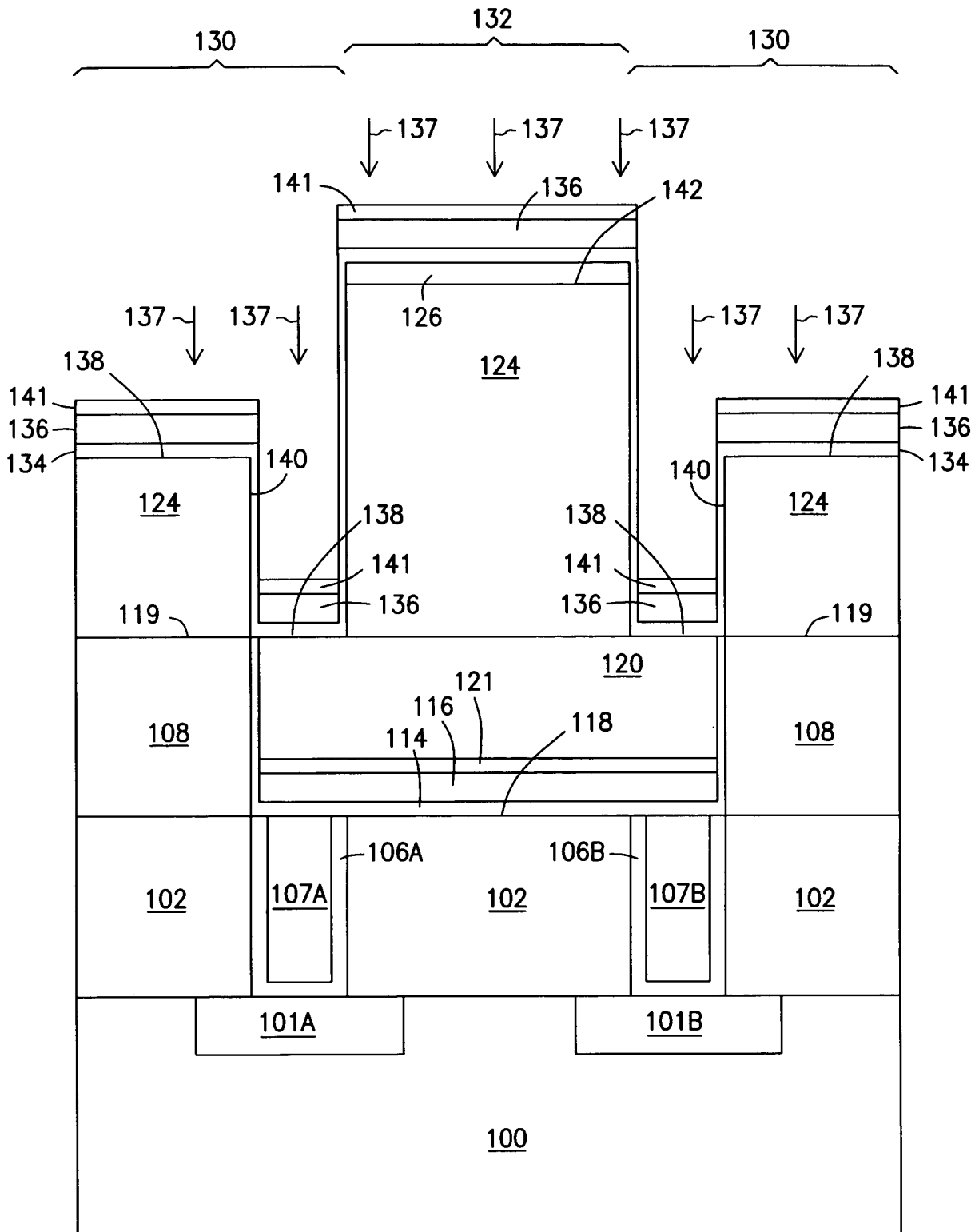


FIG. 11

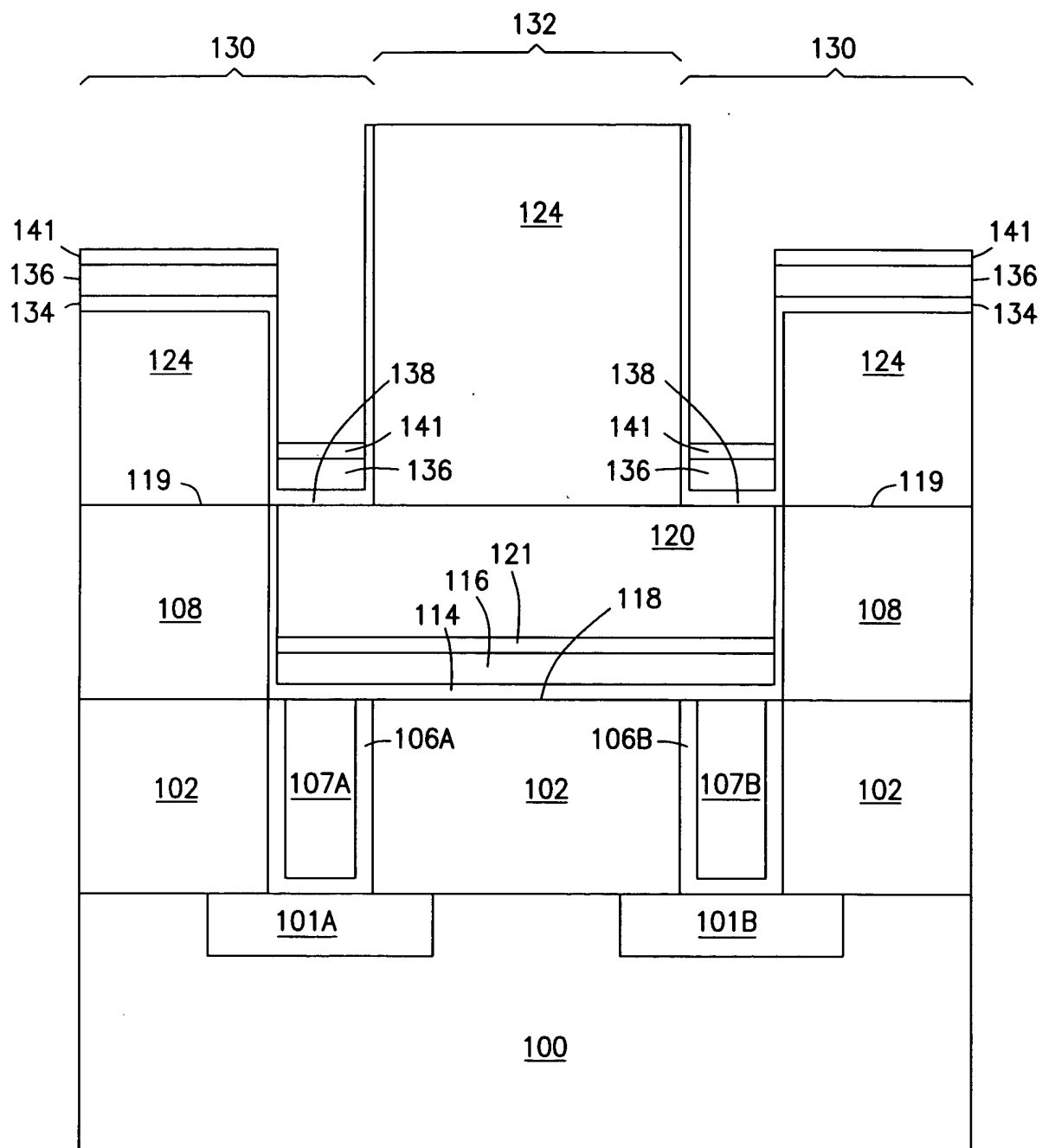


FIG. 1J

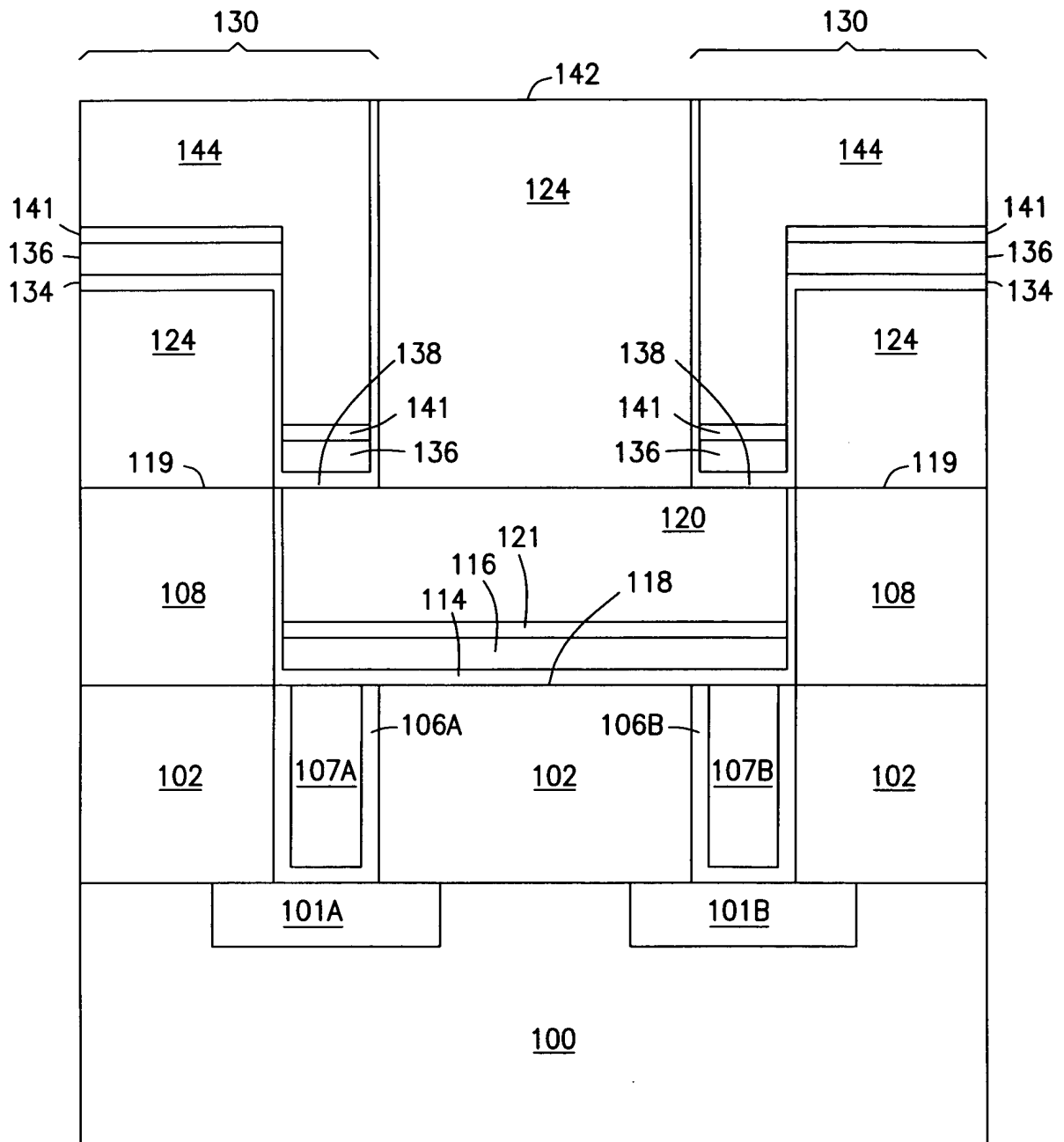


FIG. 1K

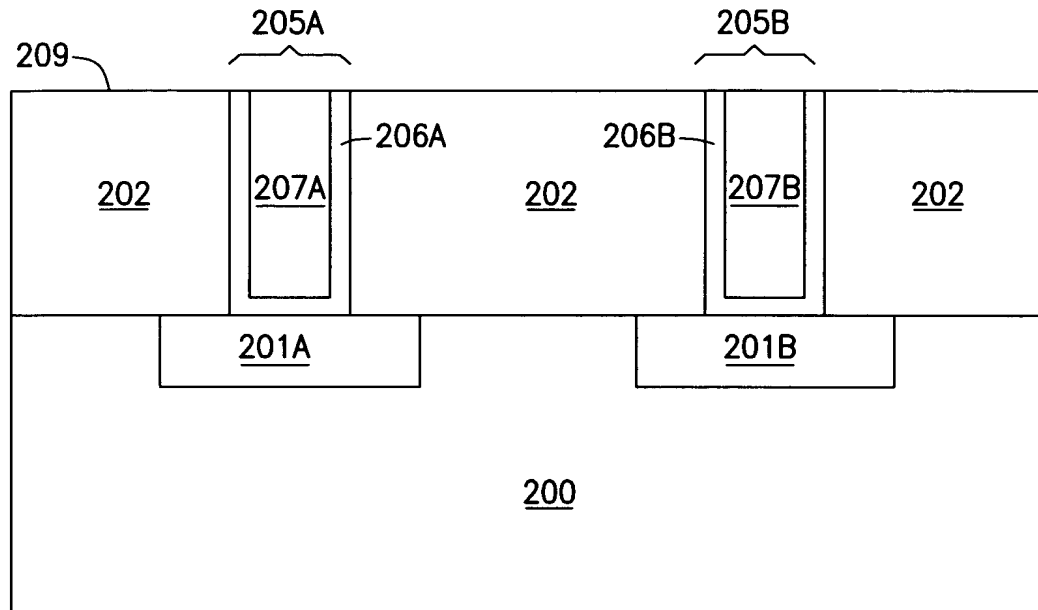


FIG. 2A

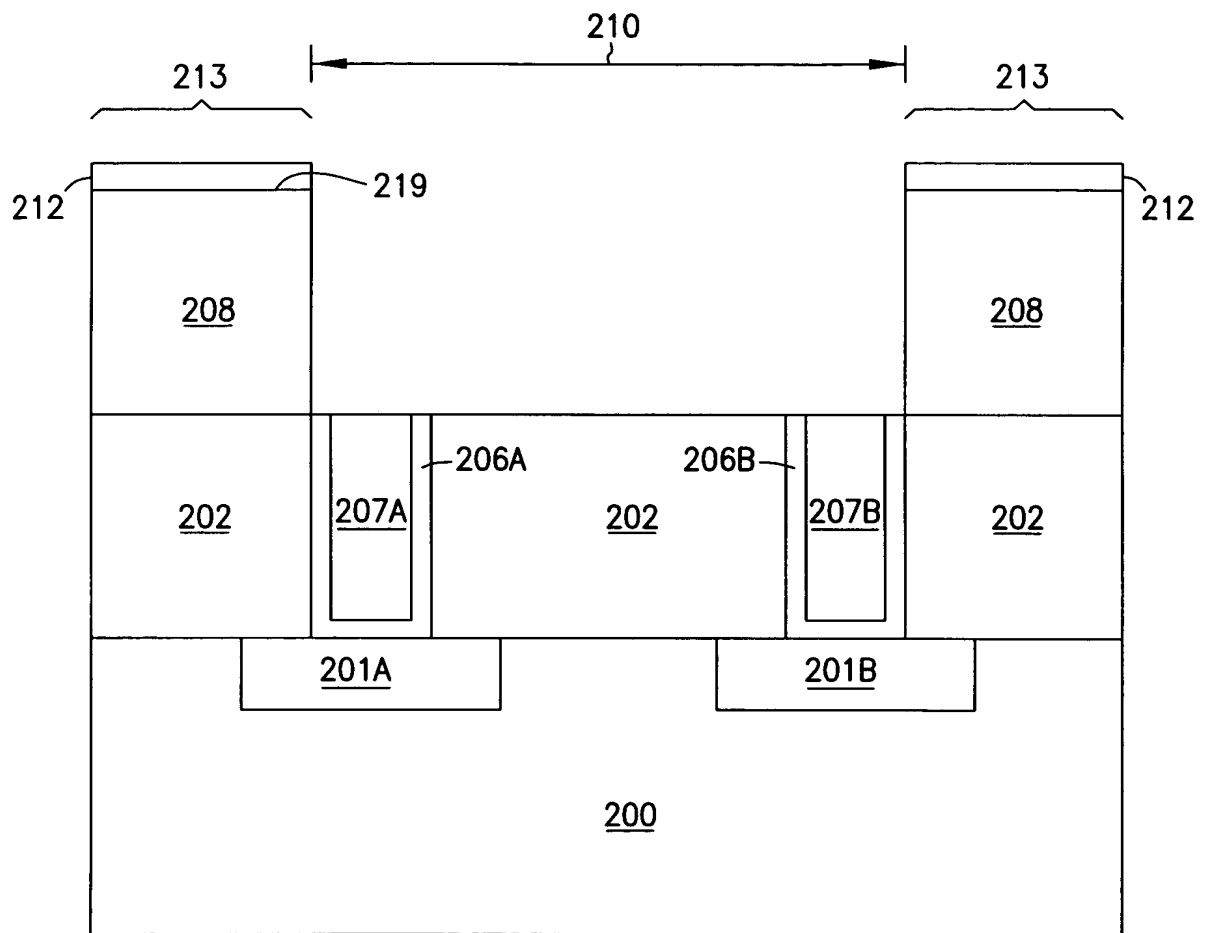


FIG. 2B

FIG. 2C



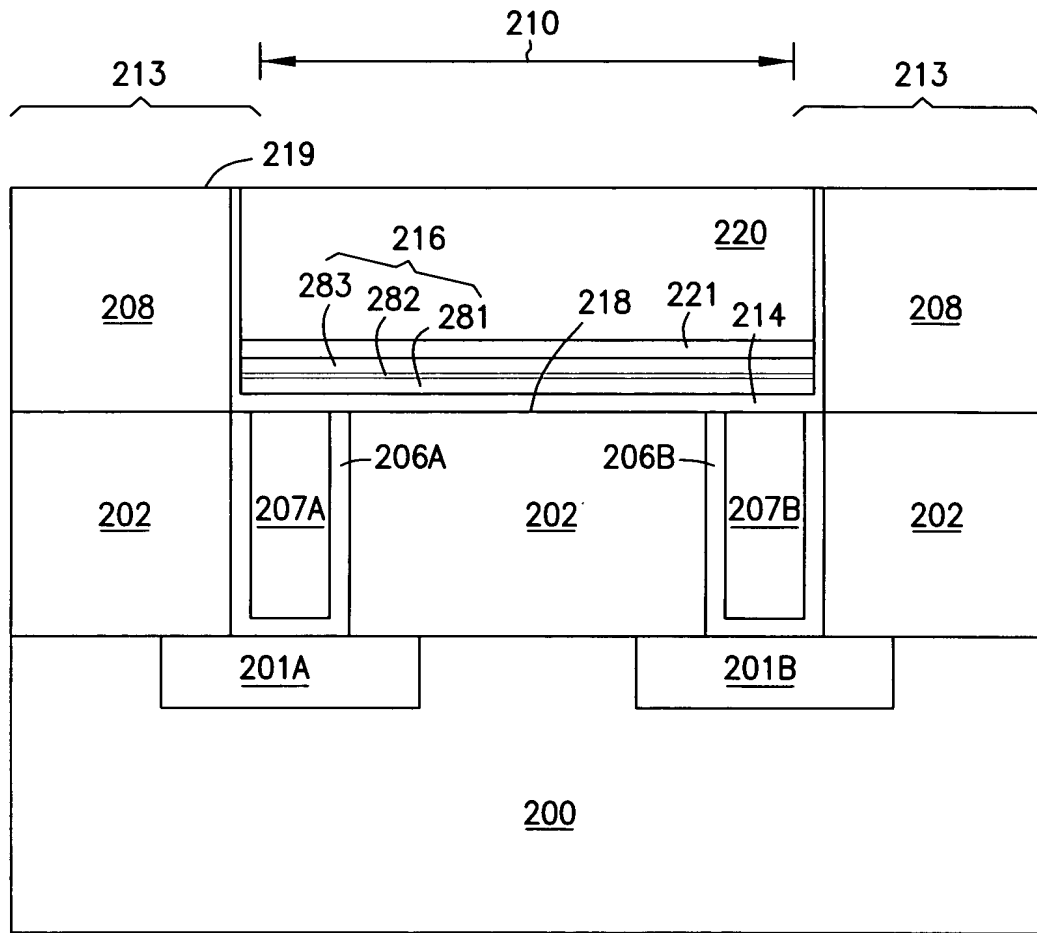


FIG. 2E



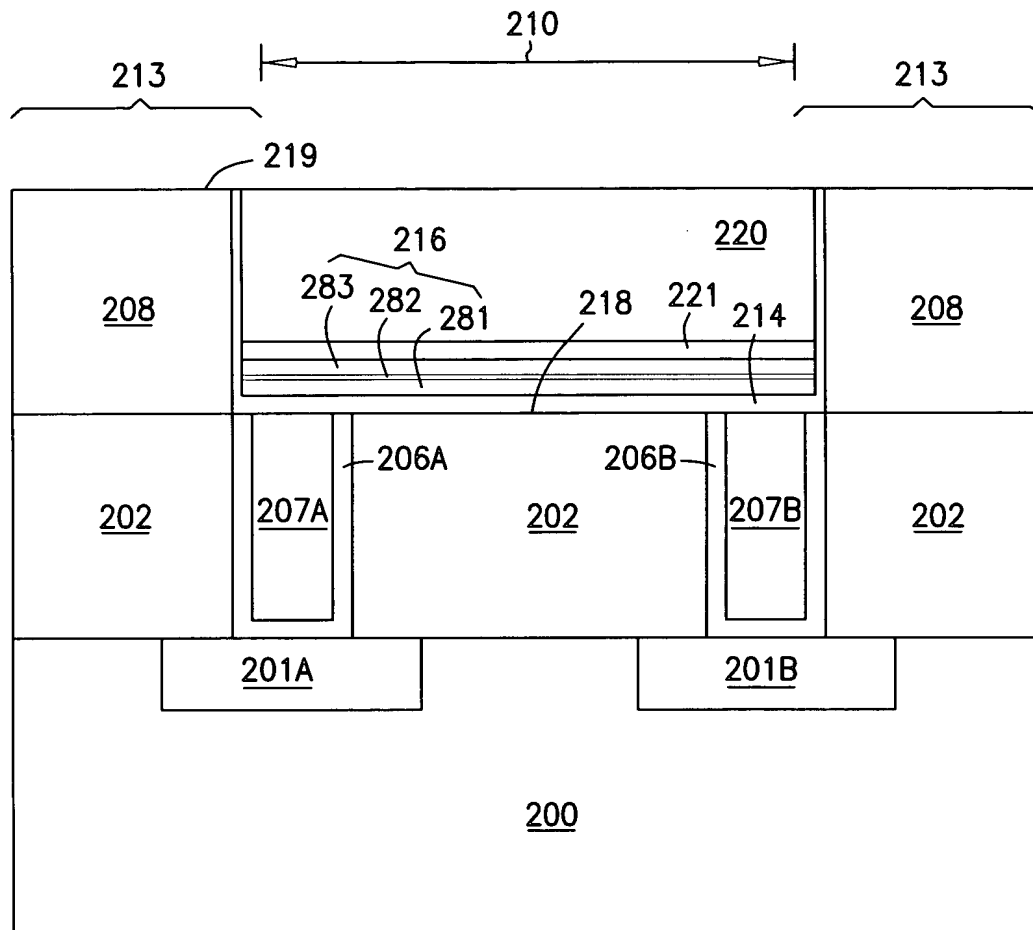


FIG. 2F



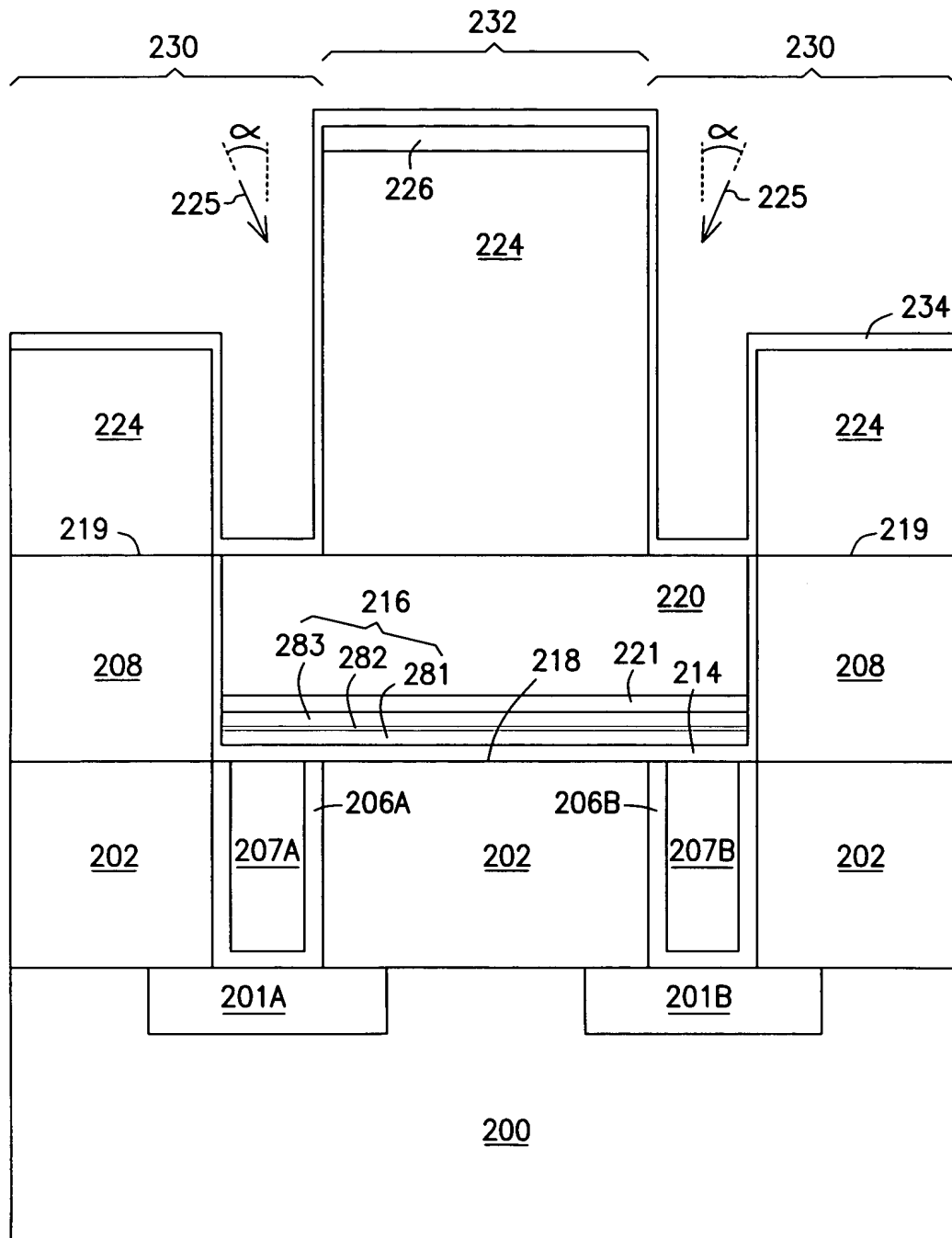


FIG. 2H

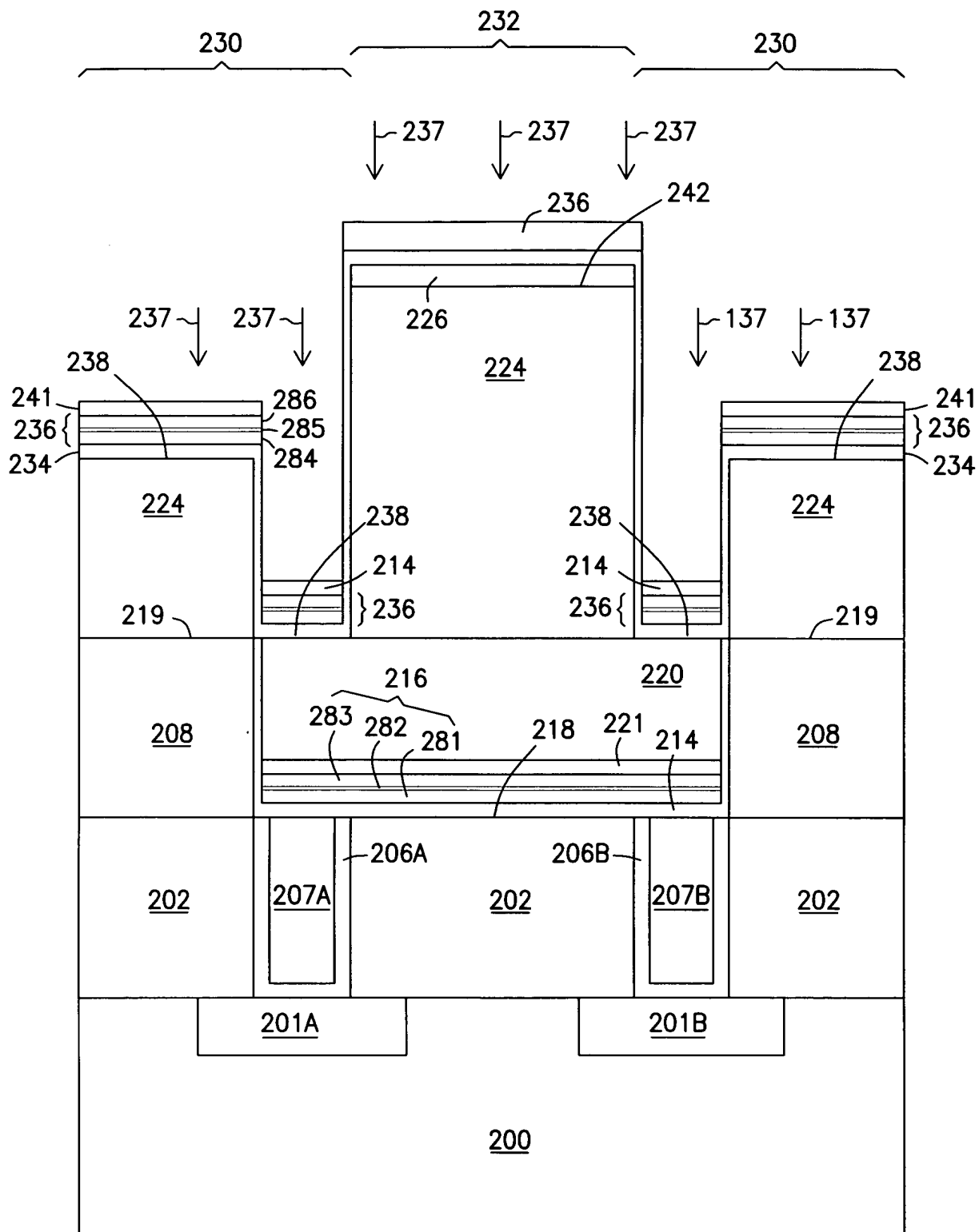


FIG. 21



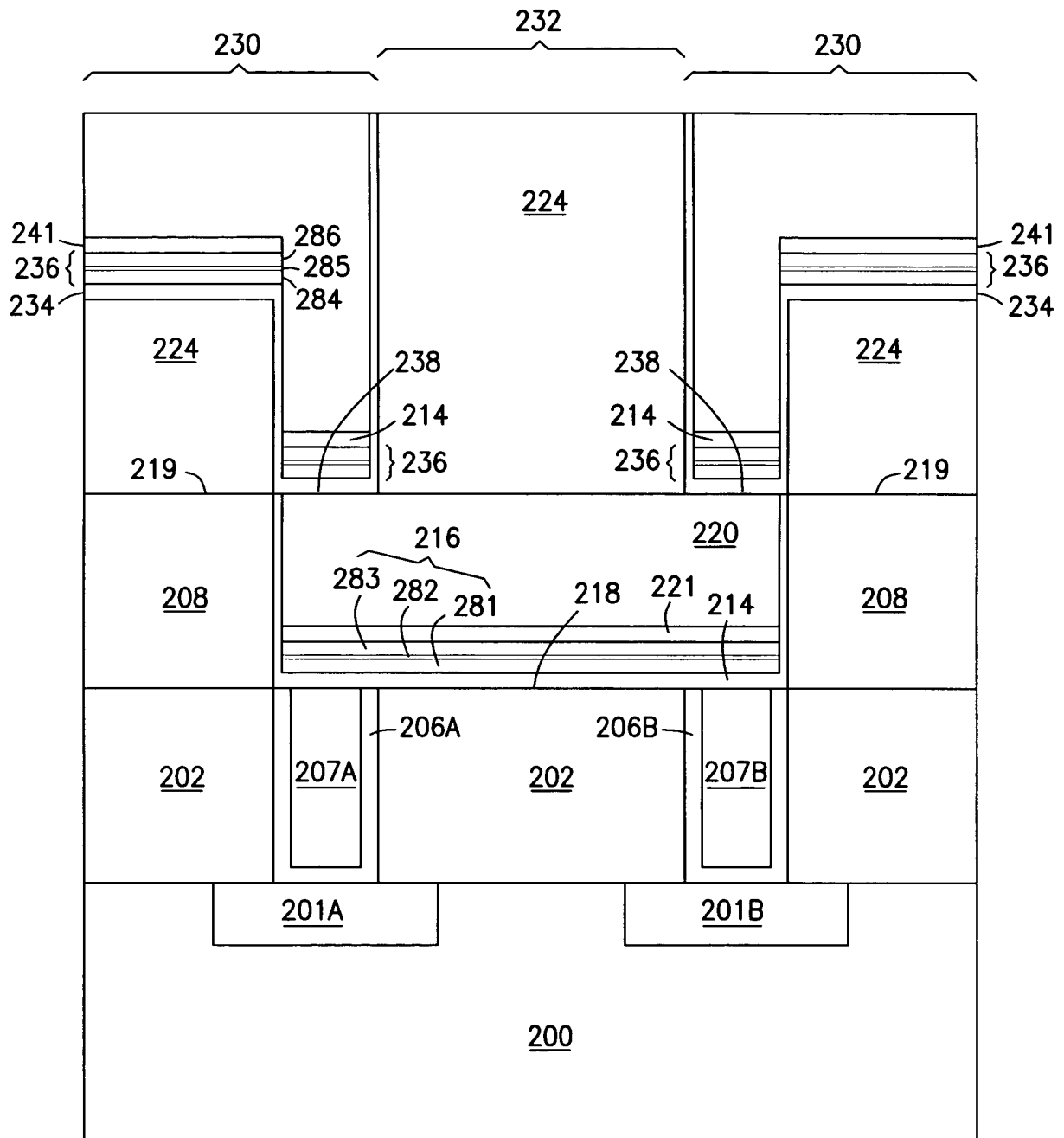


FIG. 2K

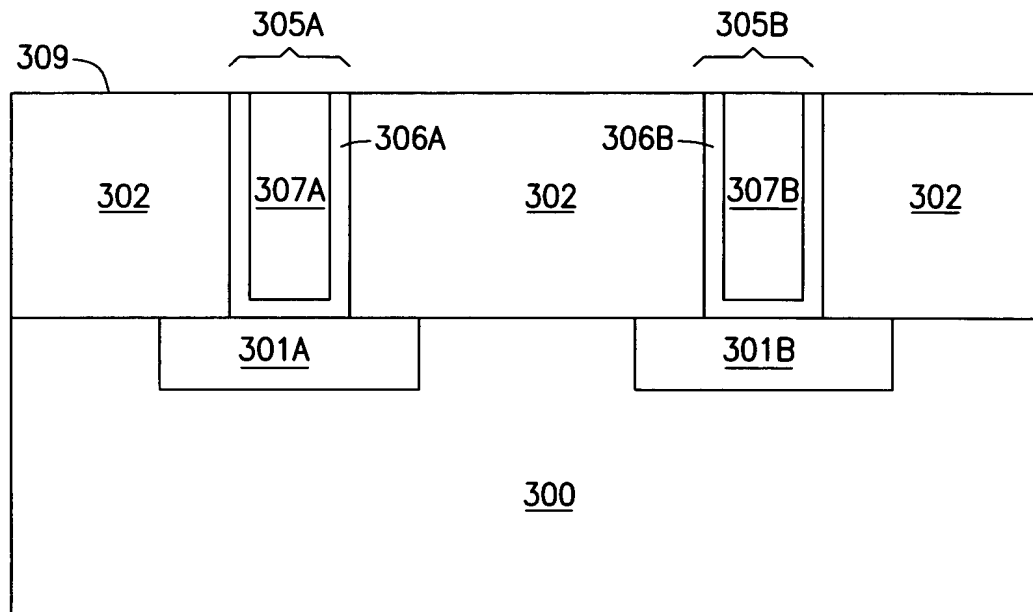


FIG. 3A

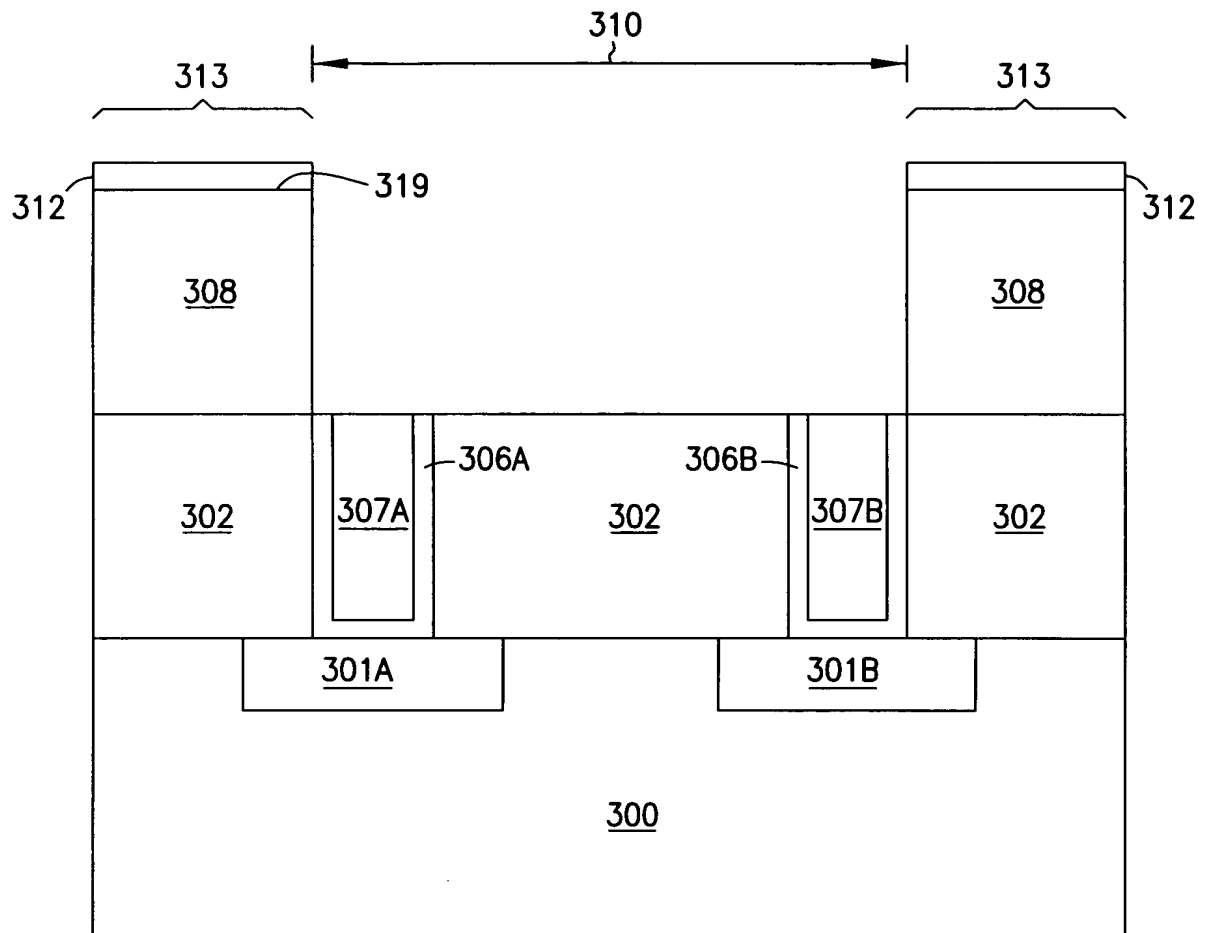


FIG. 3B





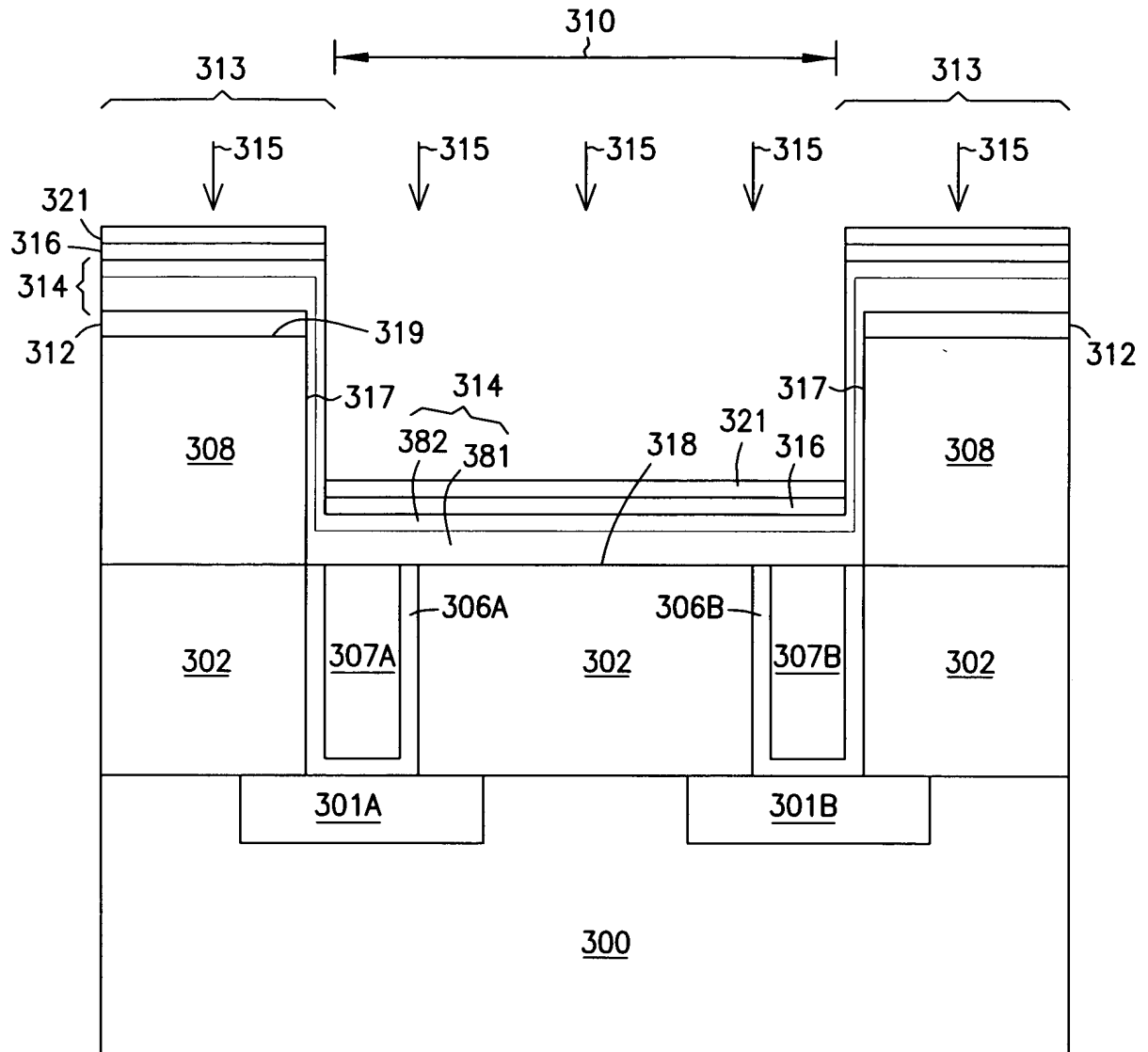


FIG. 3D

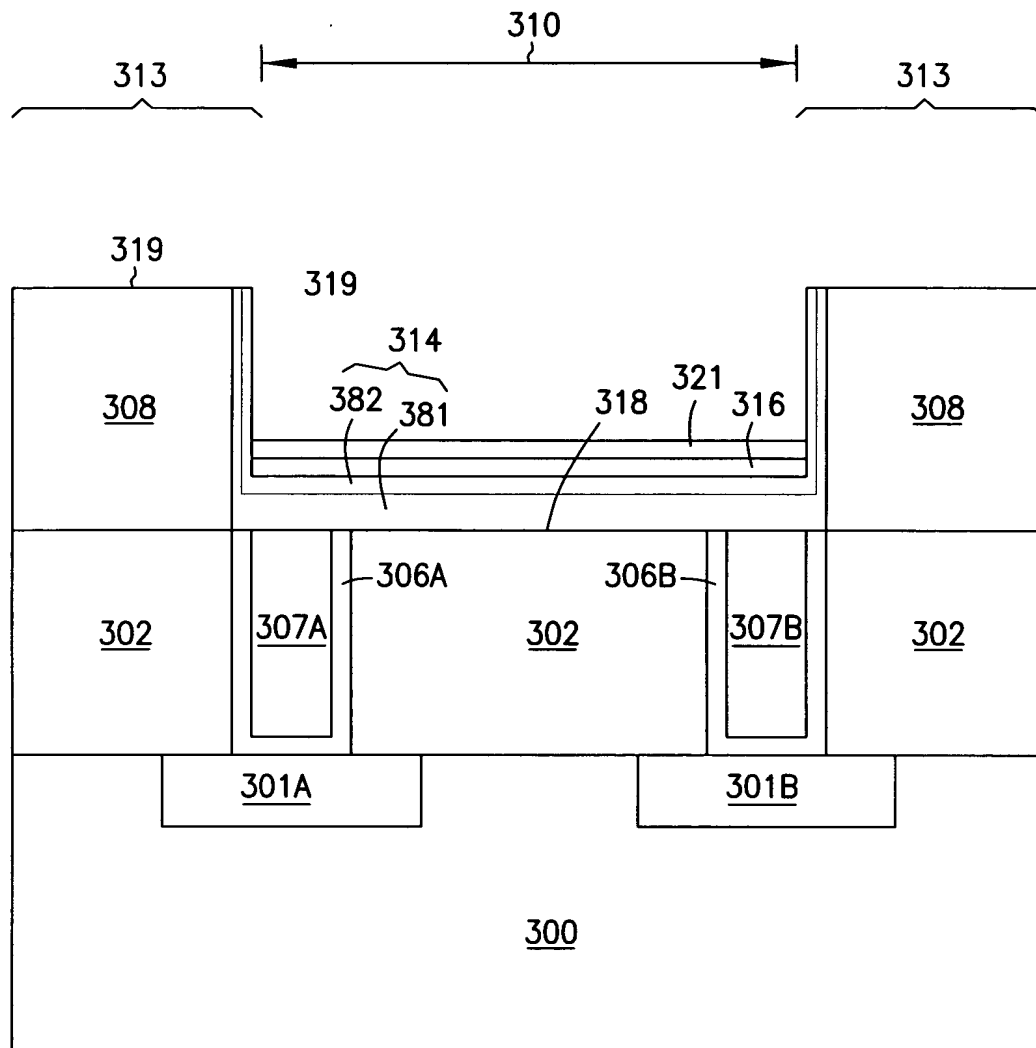


FIG. 3E

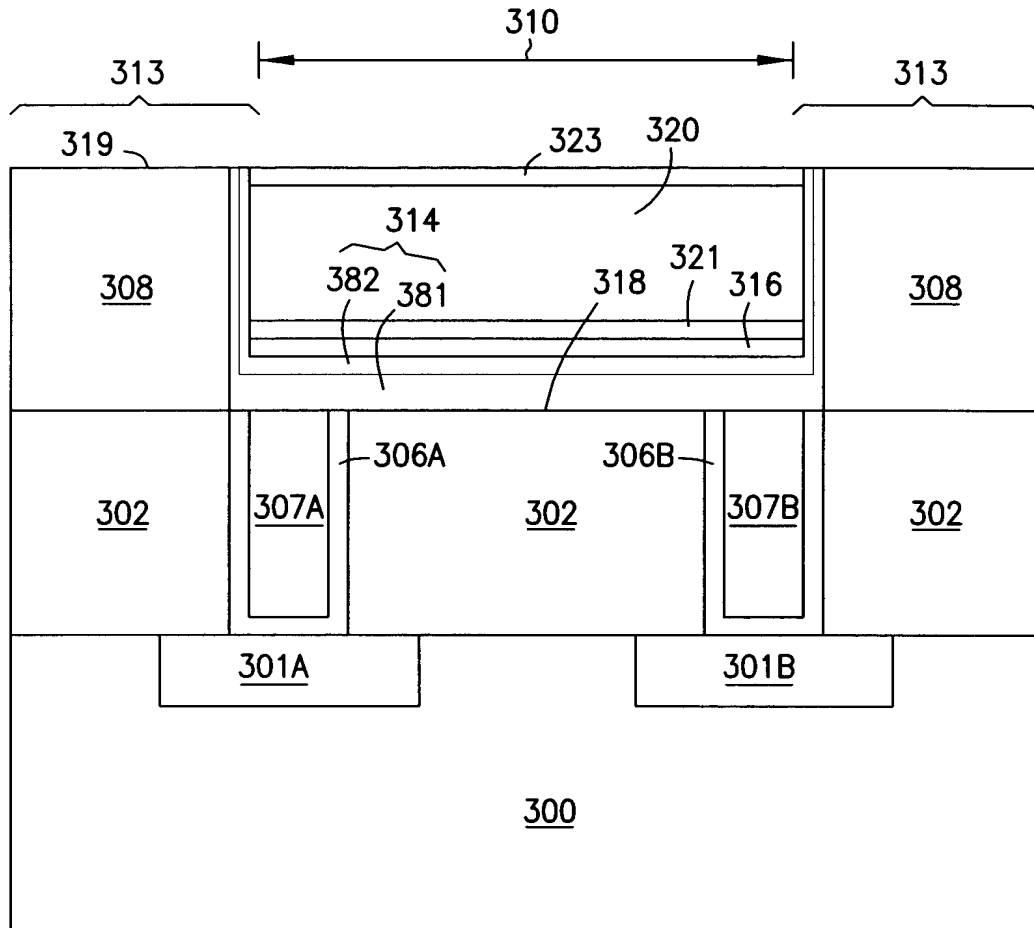


FIG. 3F

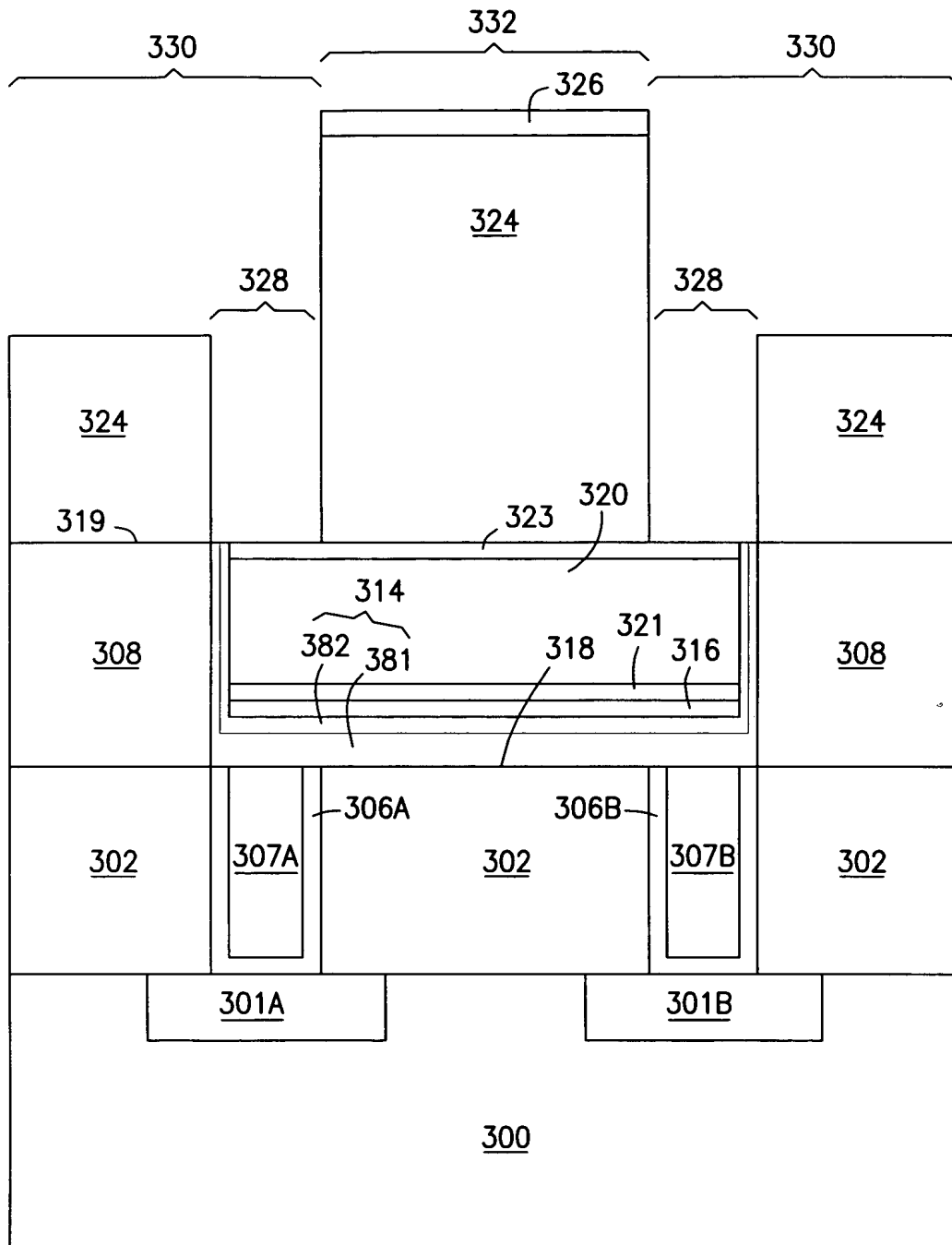


FIG. 3G



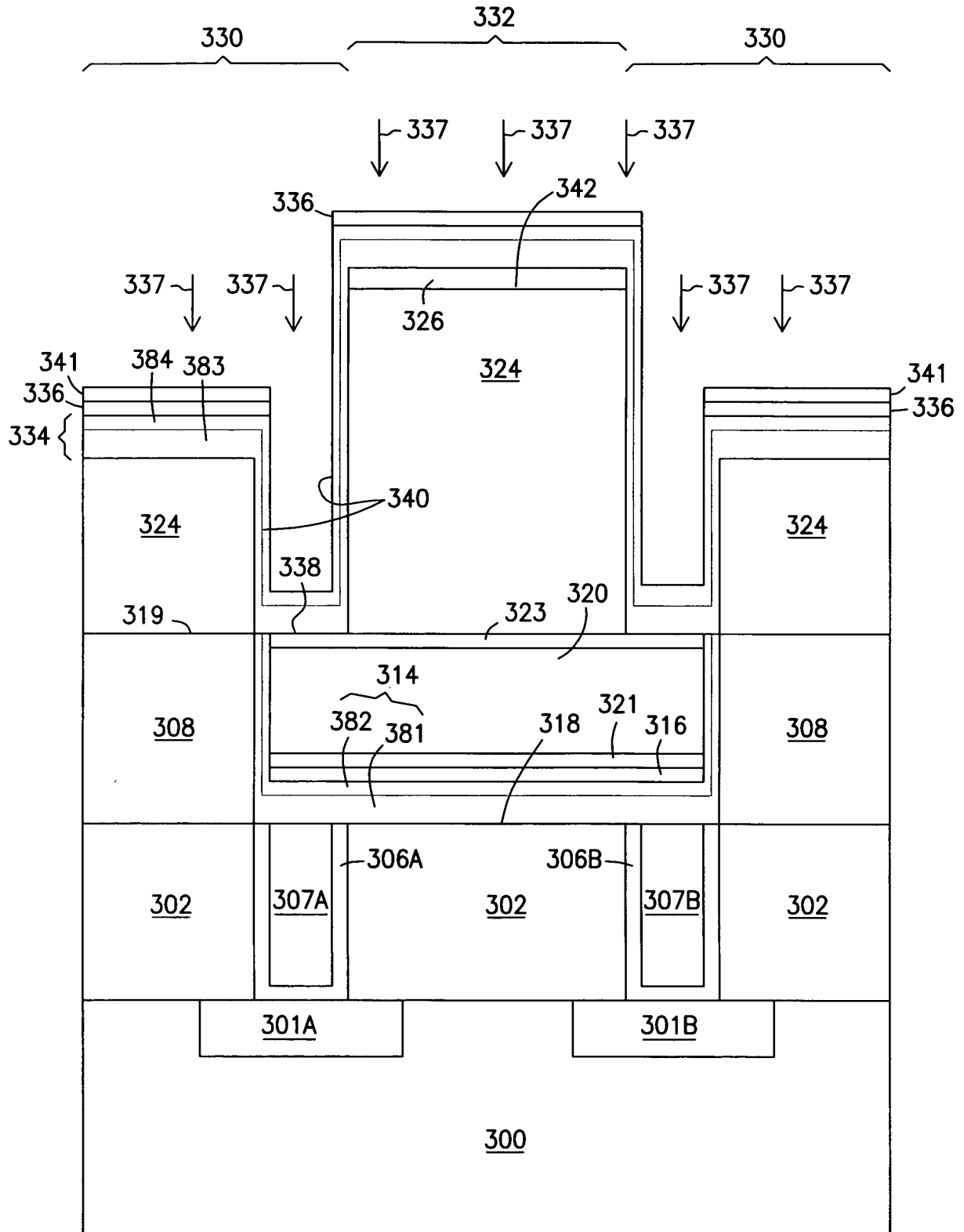


FIG. 31







FIG. 3K

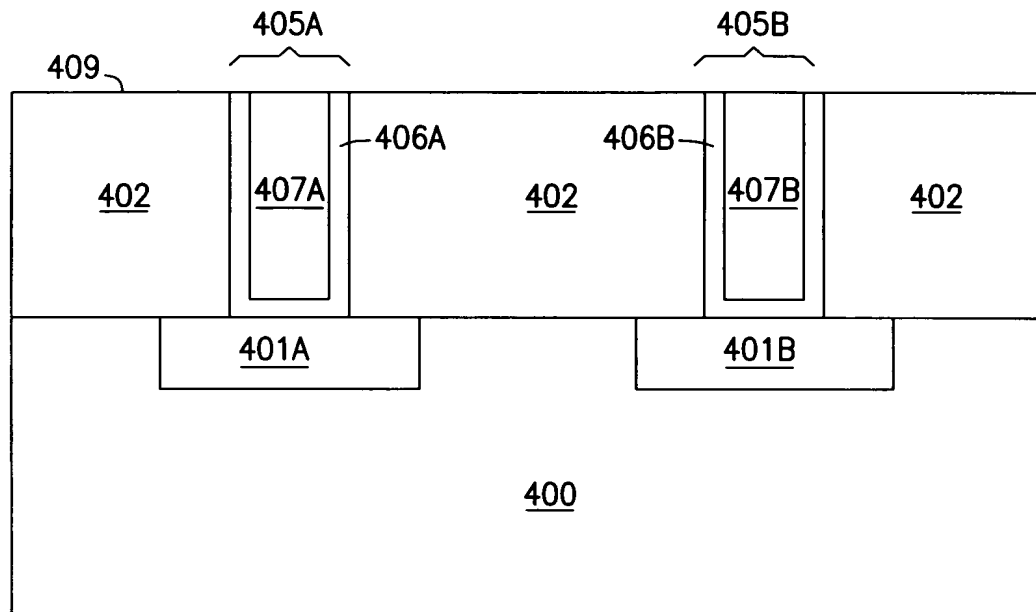


FIG. 4A

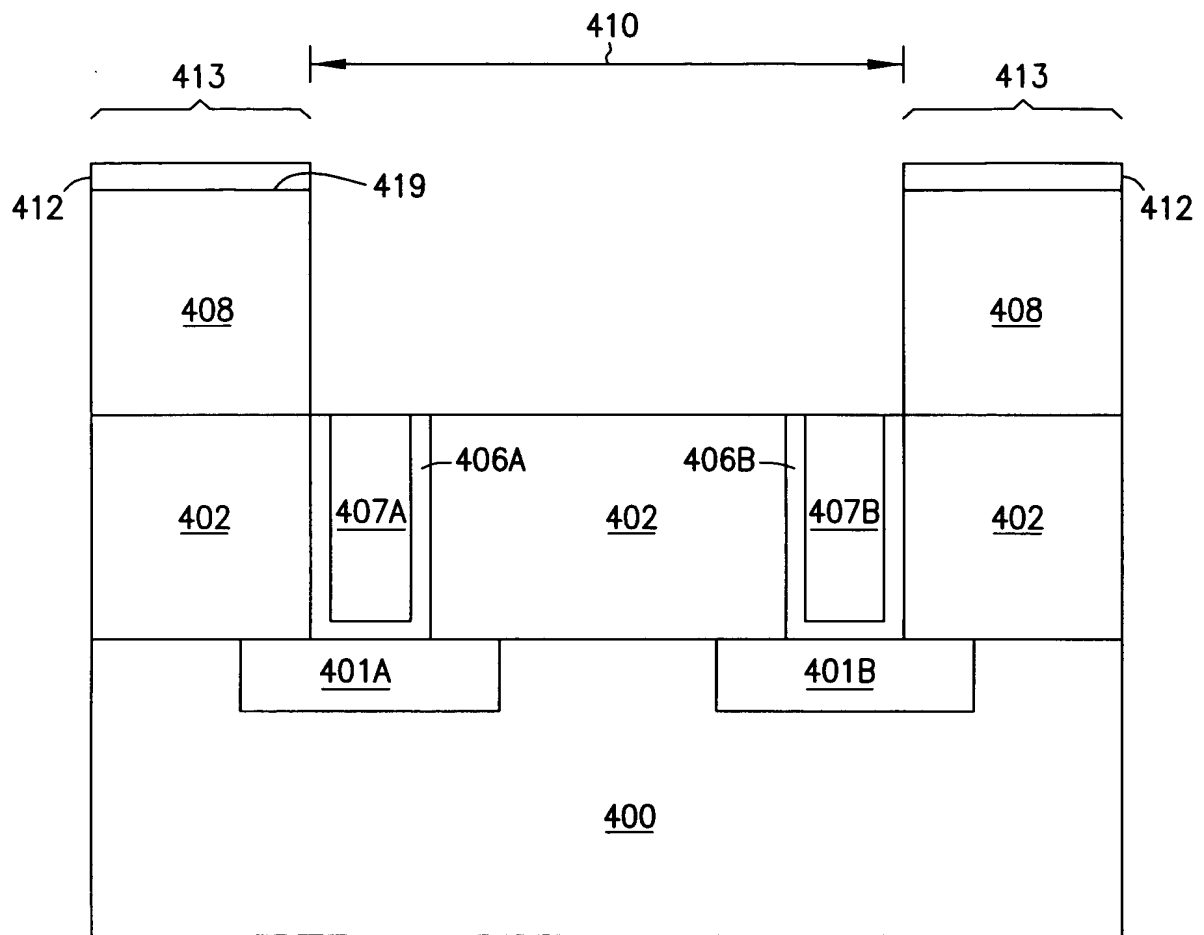


FIG. 4B

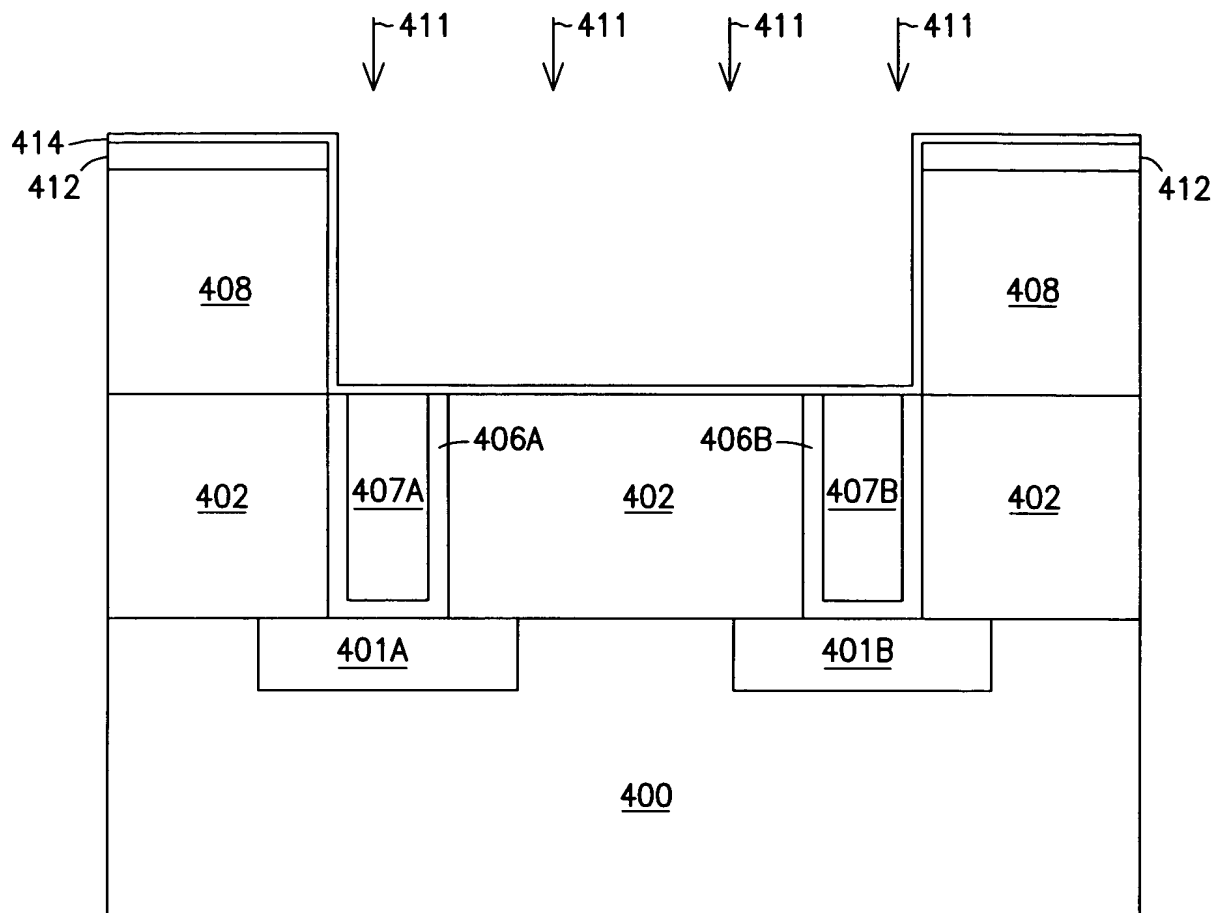


FIG. 4C

FIG. 4D

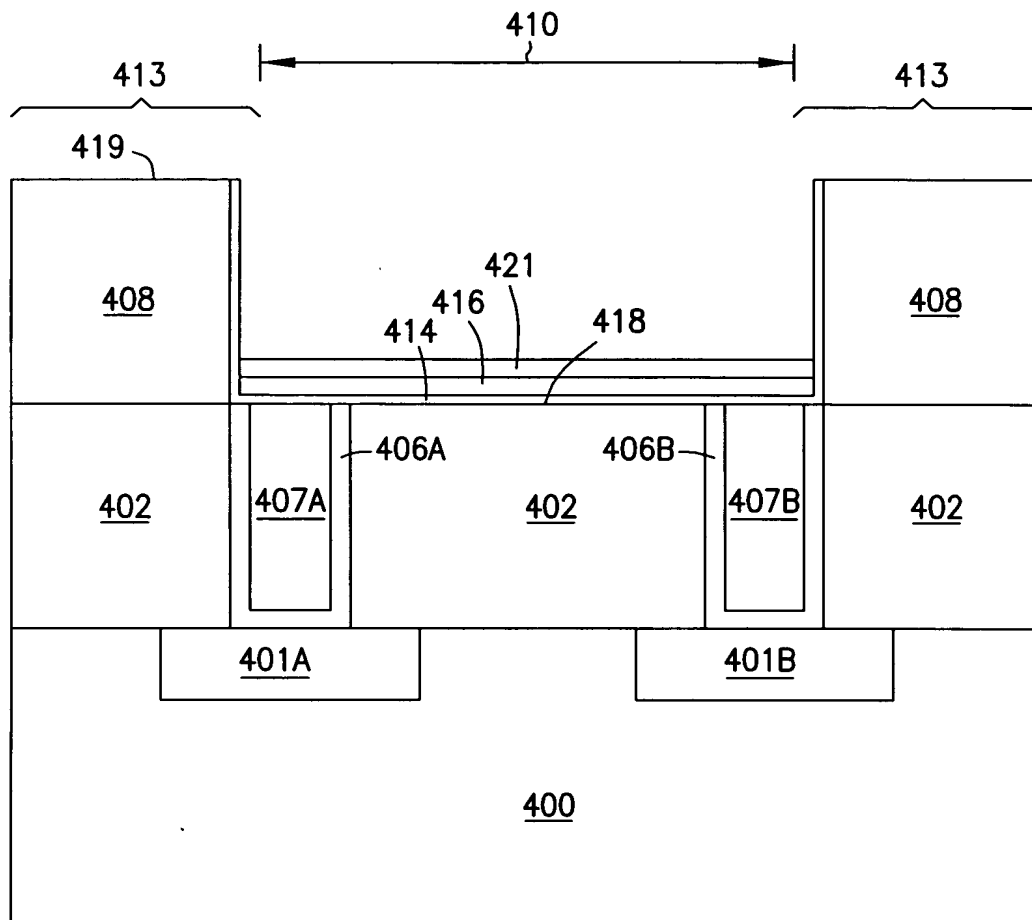


FIG. 4E

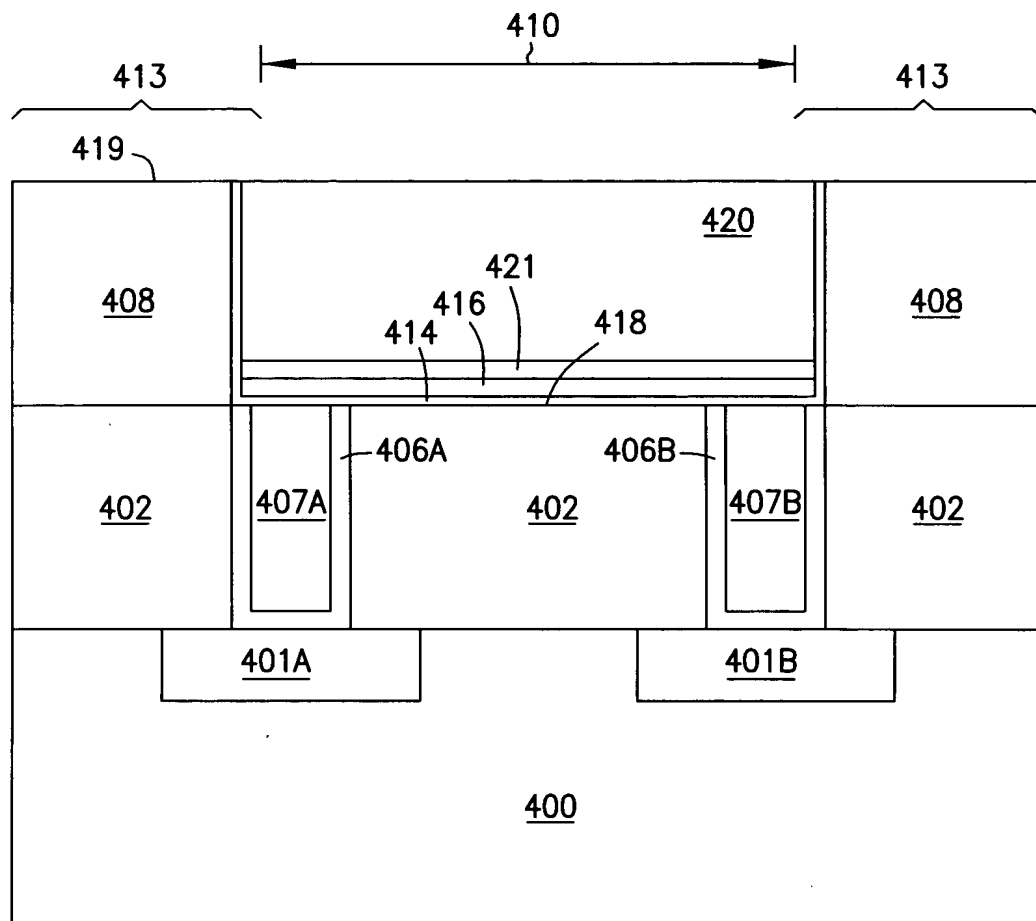


FIG. 4F

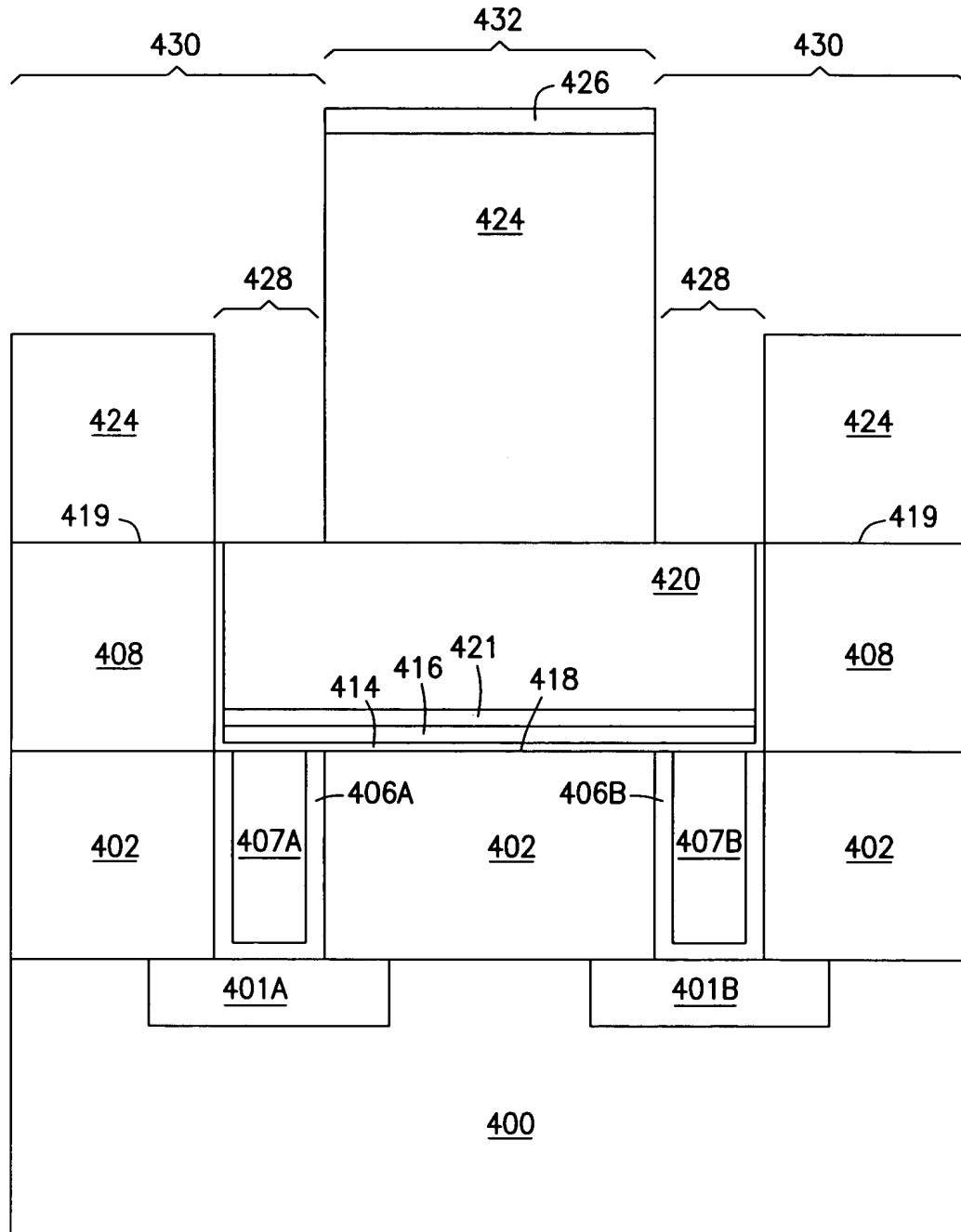


FIG. 4G



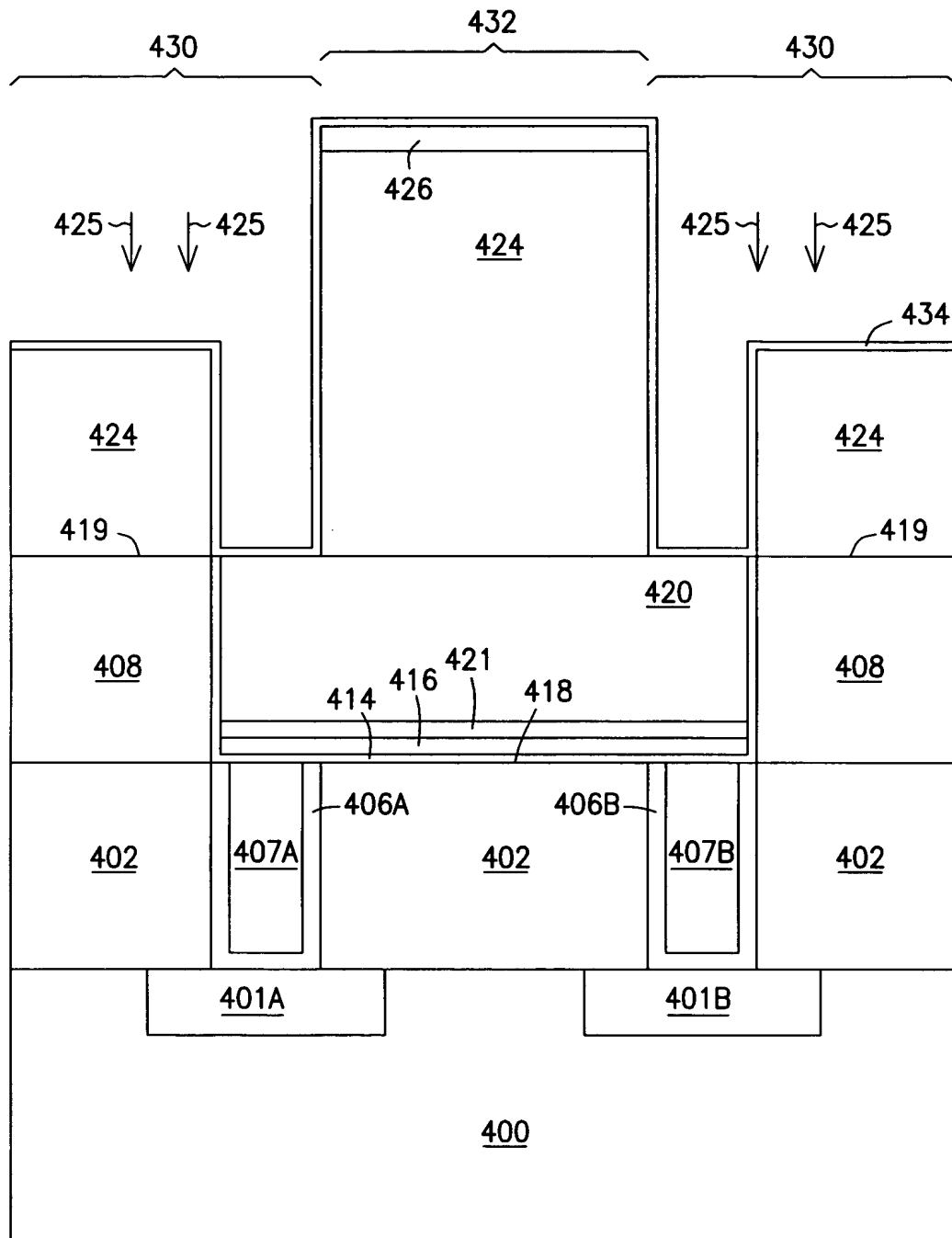


FIG. 4H

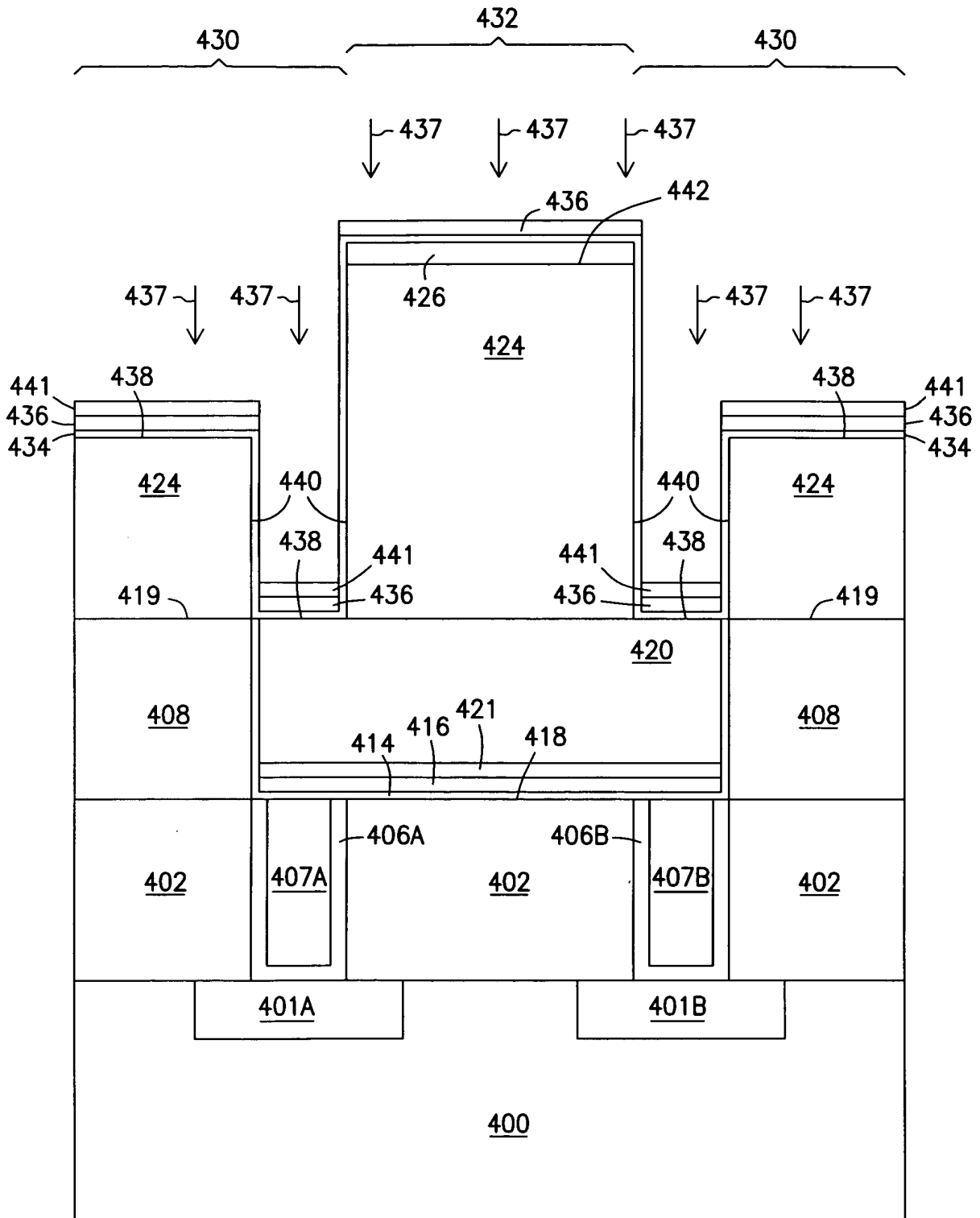


FIG. 4I

FIG. 4J

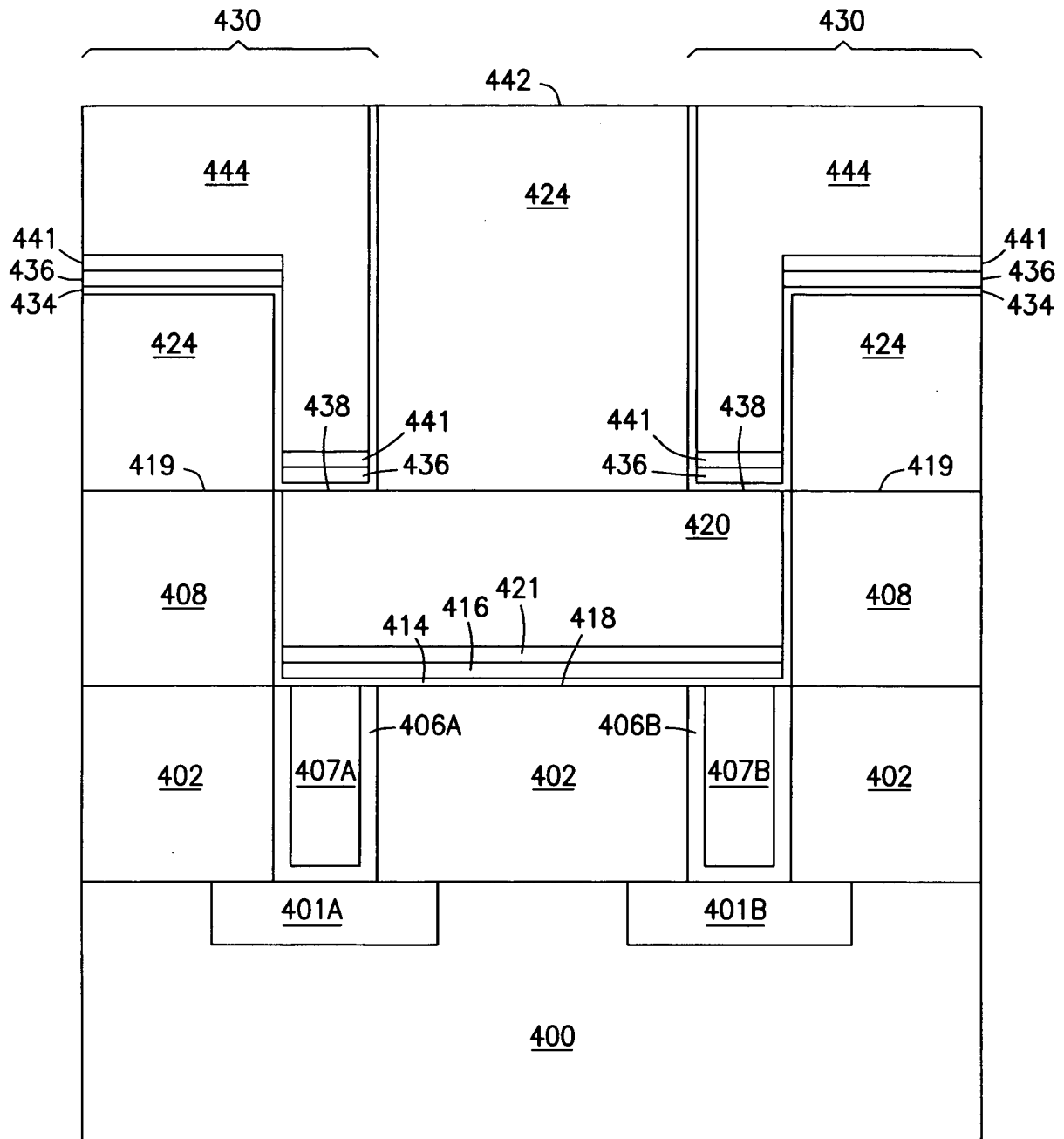


FIG. 4K

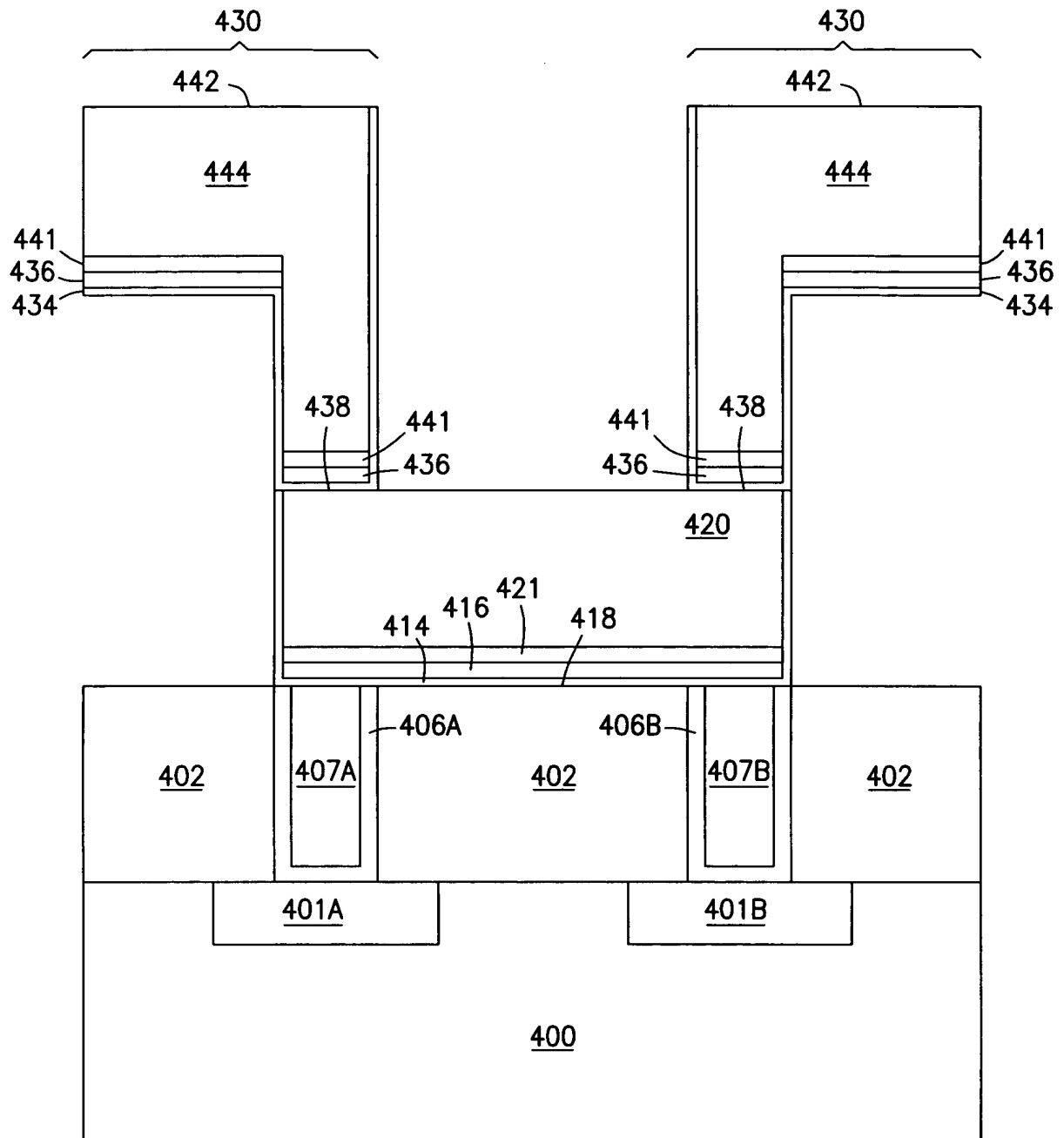


FIG. 4L

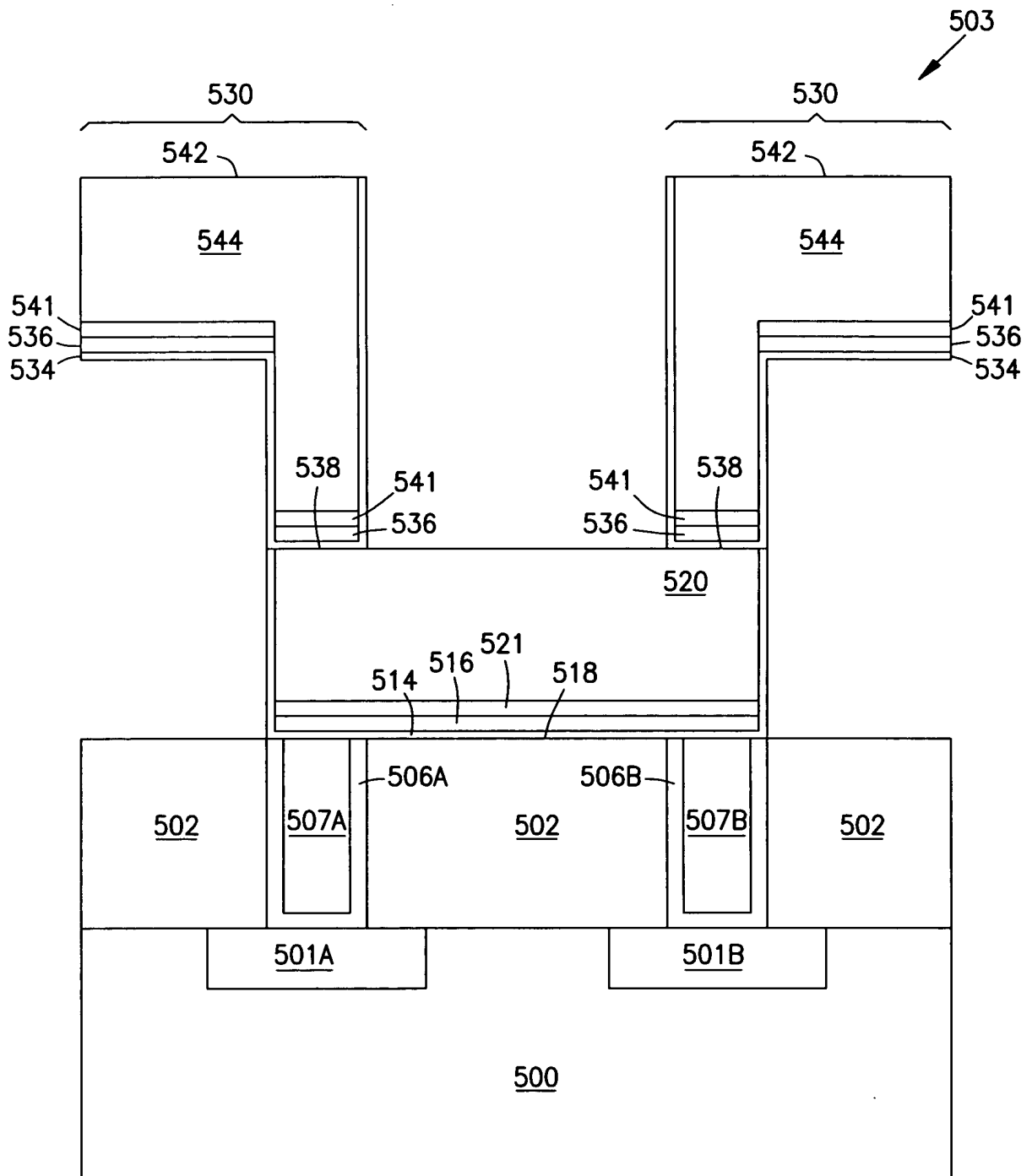


FIG. 5

TITLE: INTEGRATED CIRCUIT AND SEED LAYERS

INVENTORS NAME: Paul A. Farrar

DOCKET NO.: 303.673US3

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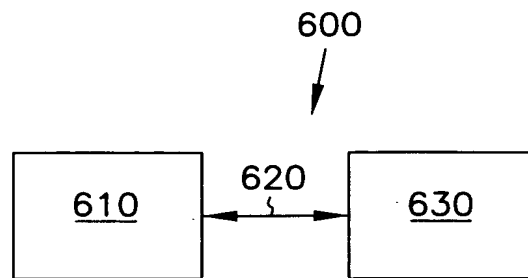


FIG. 6